

Model Name: GA-Z68MX-UD2H

Revision 1.3

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2011/07/19

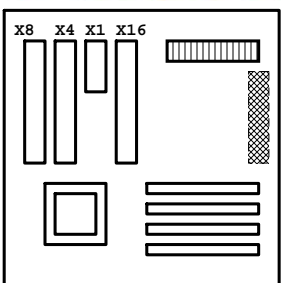
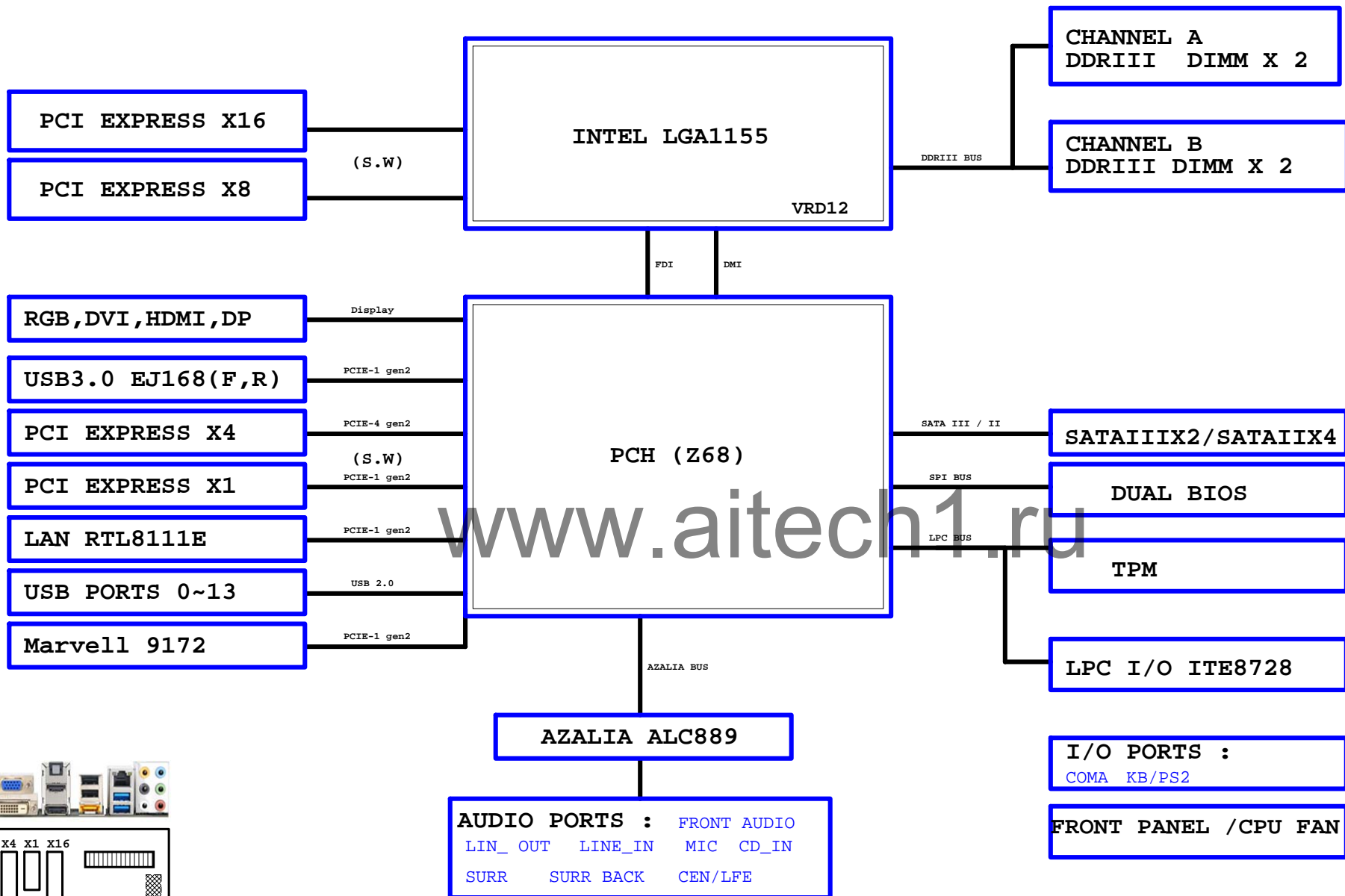
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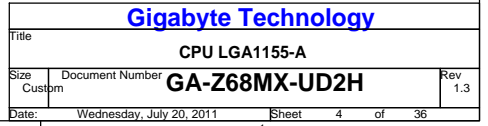
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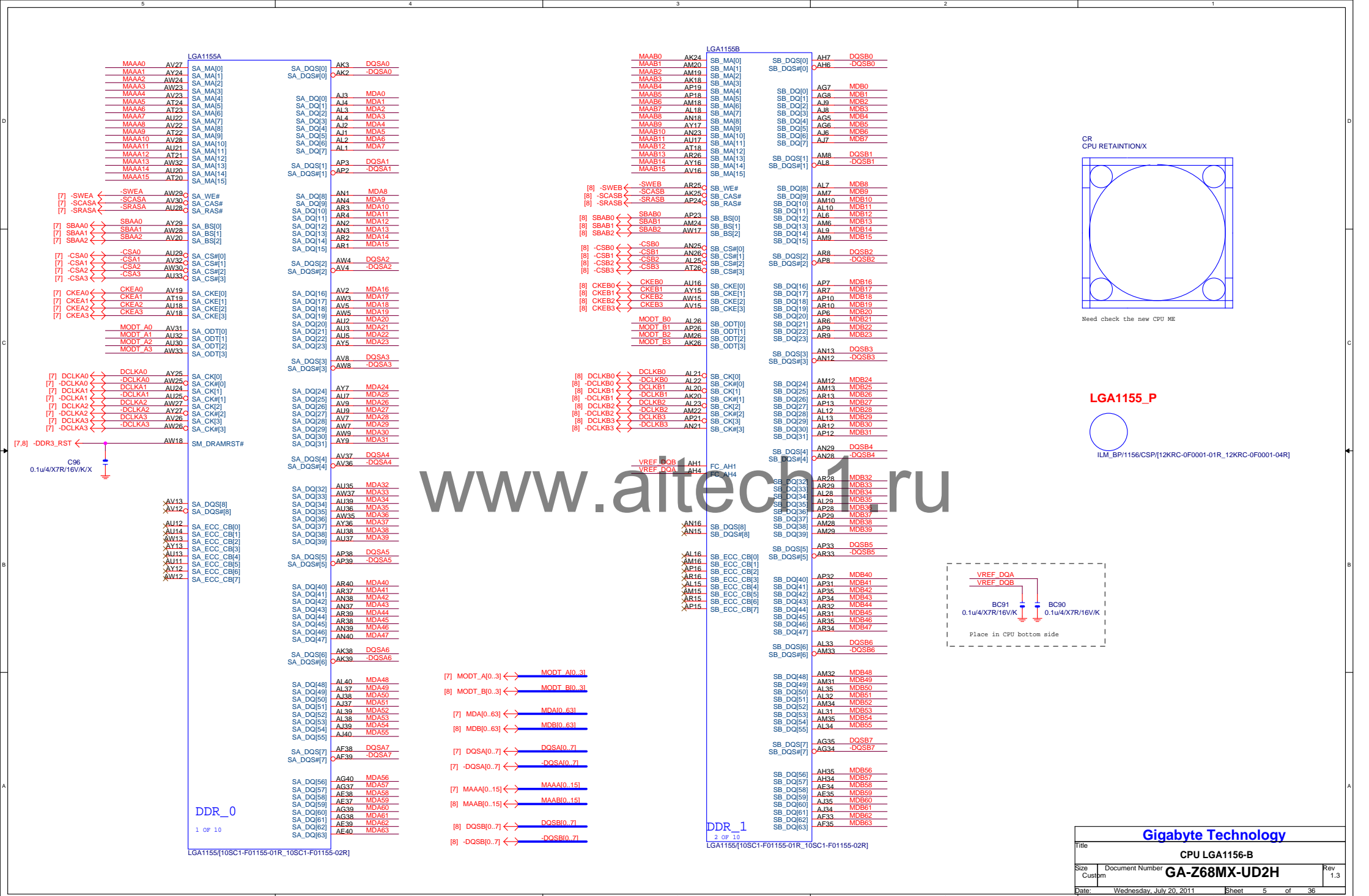
Title	BOM & PCB MODIFY HISTORY
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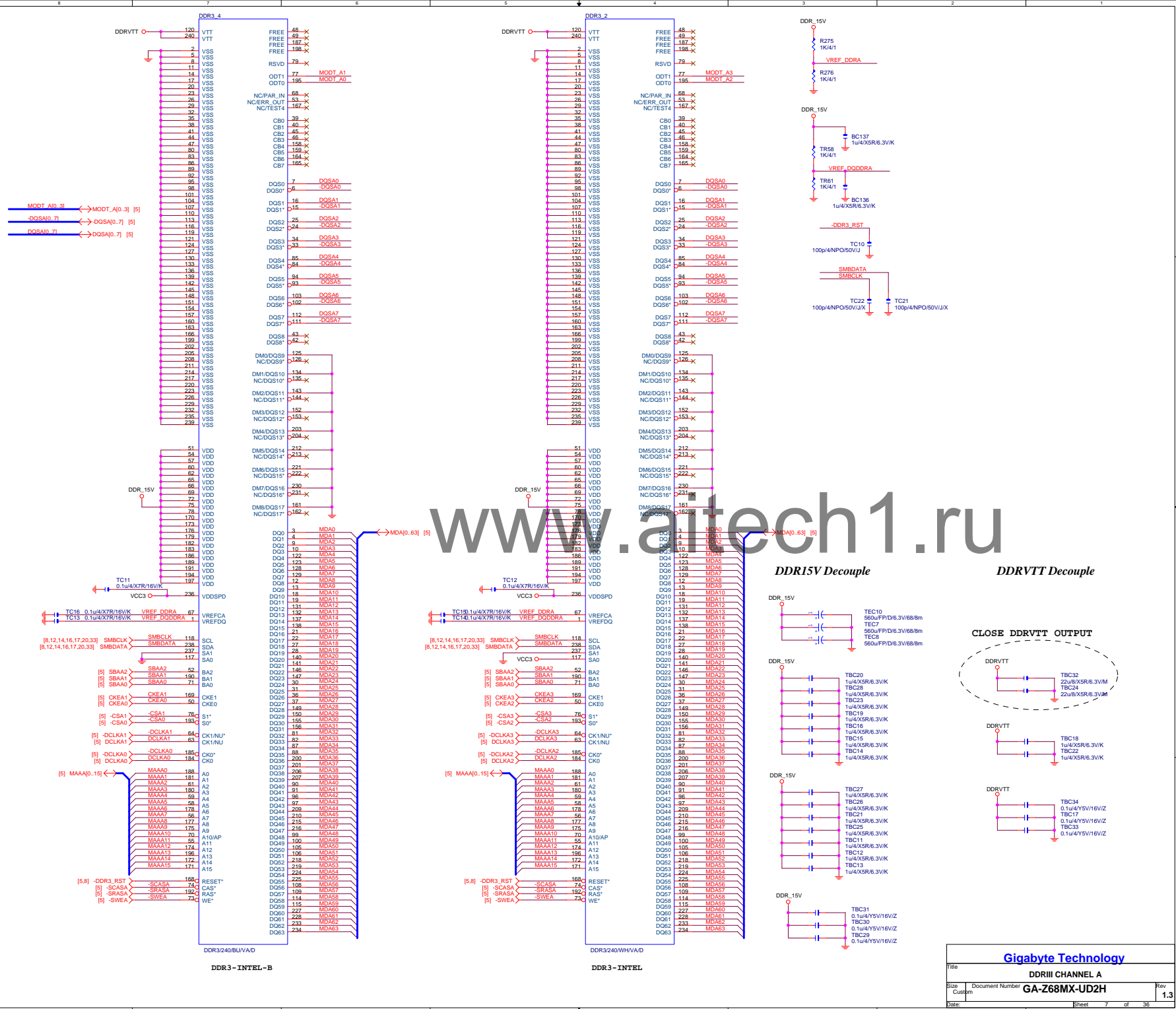
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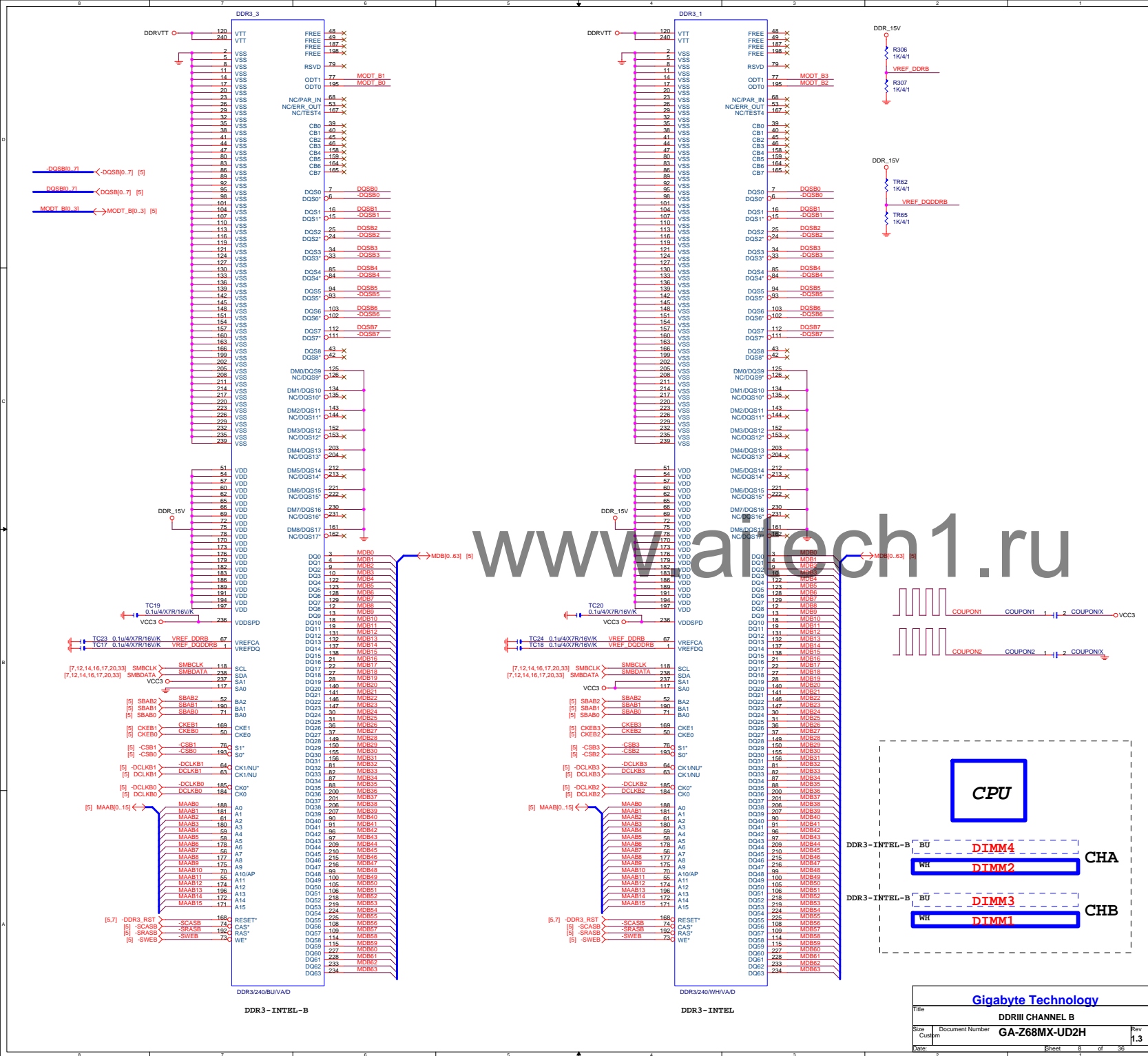
BLOCK DIAGRAM

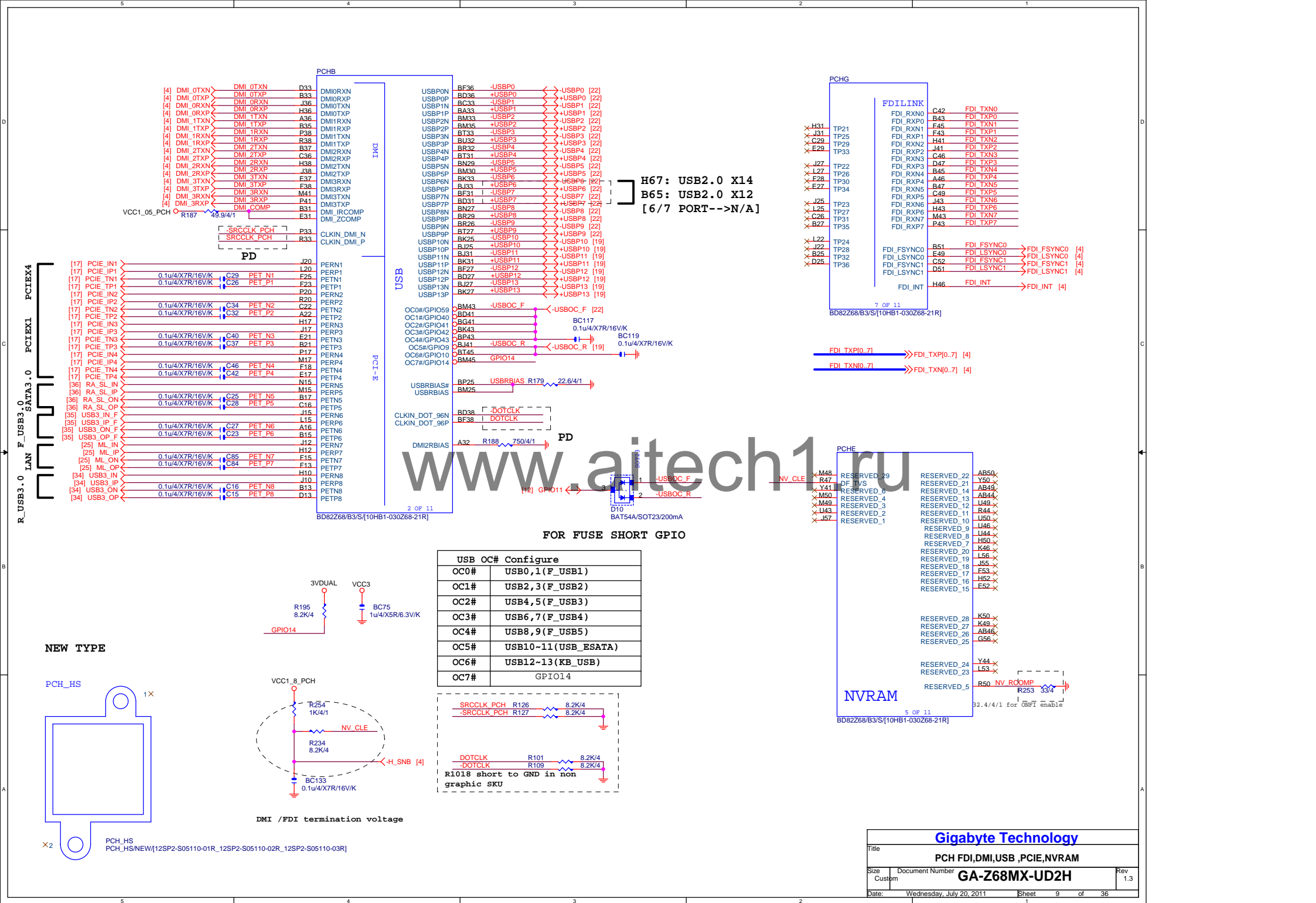




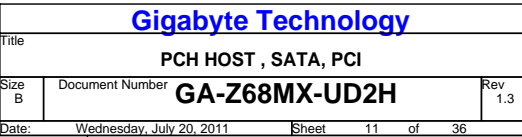


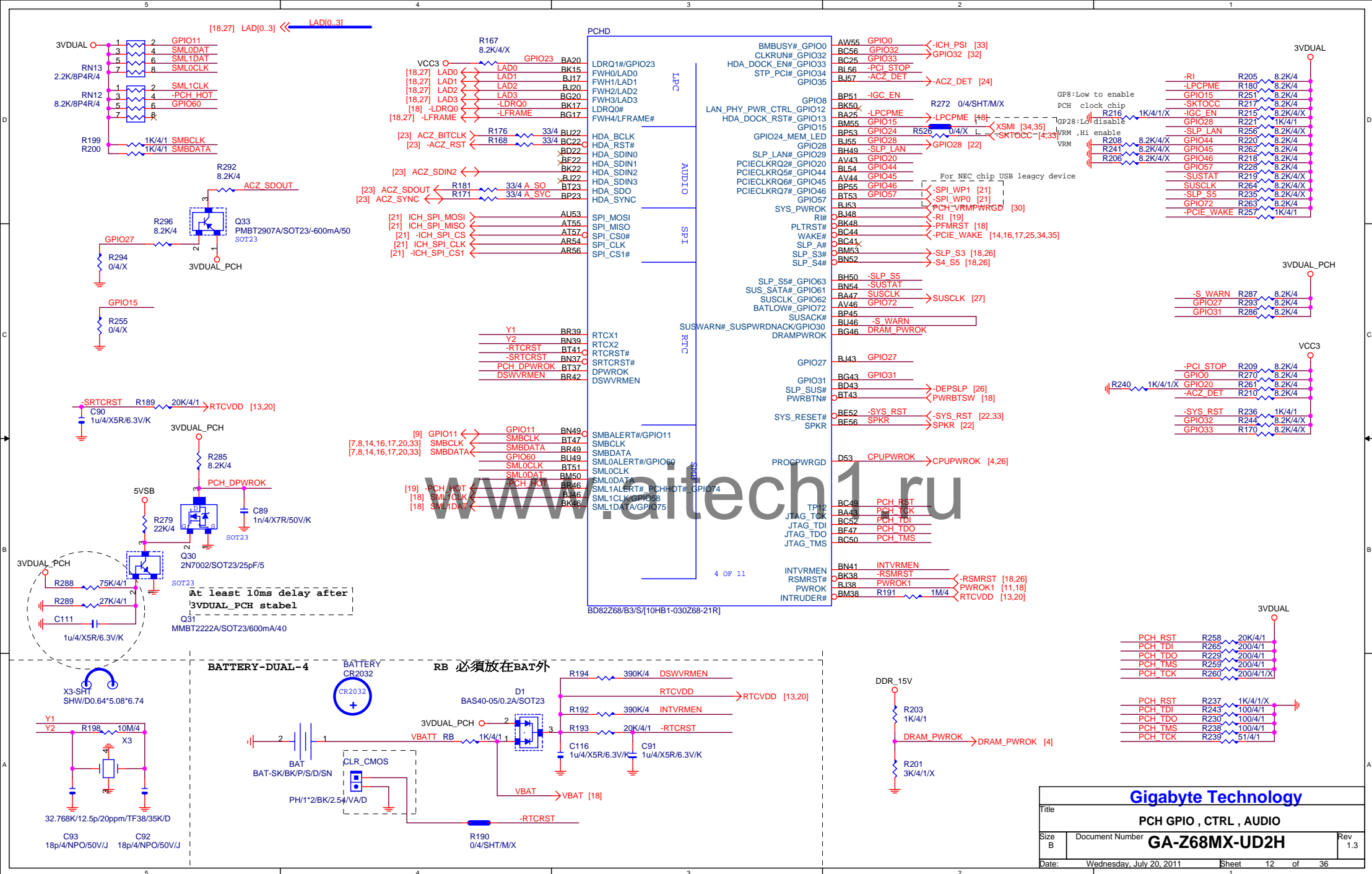


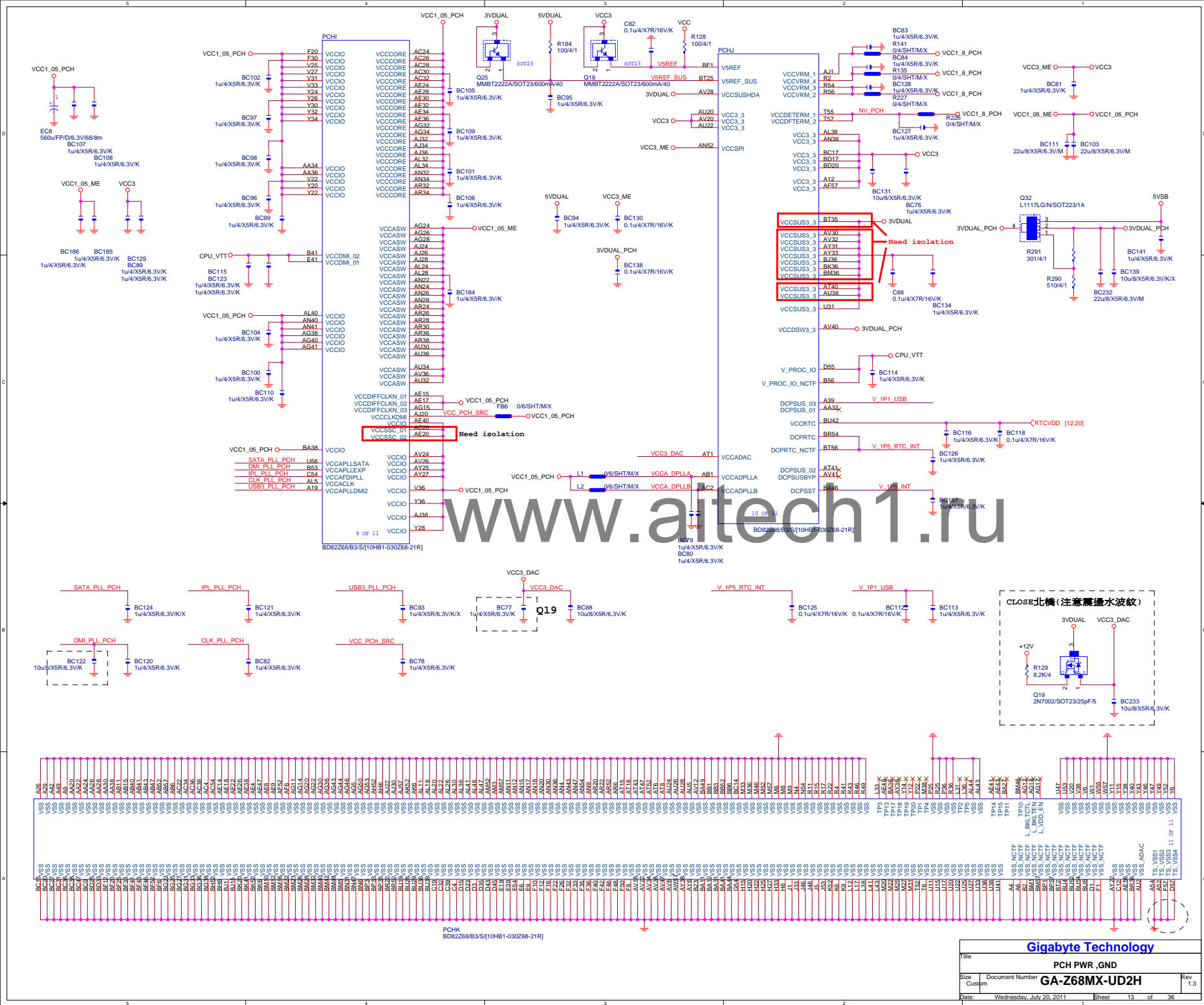




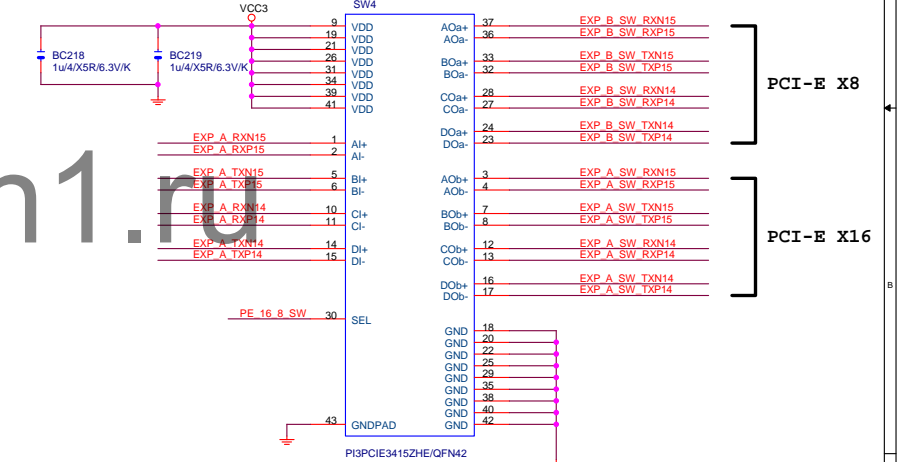
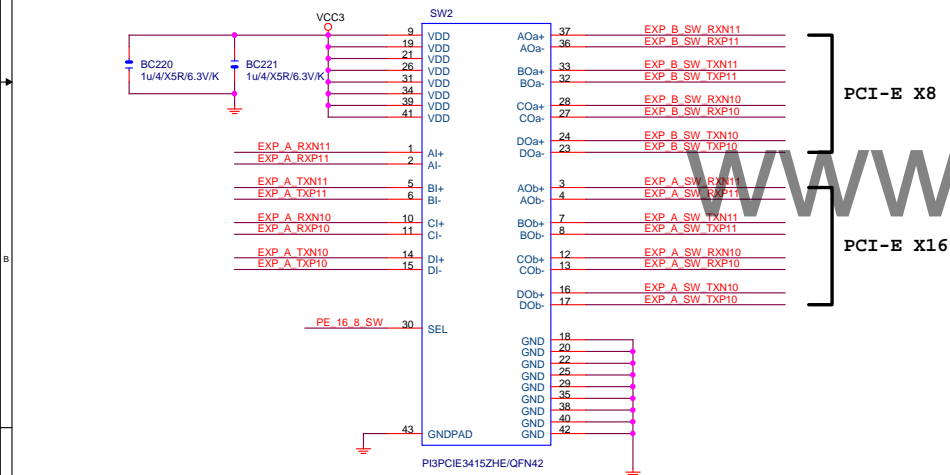
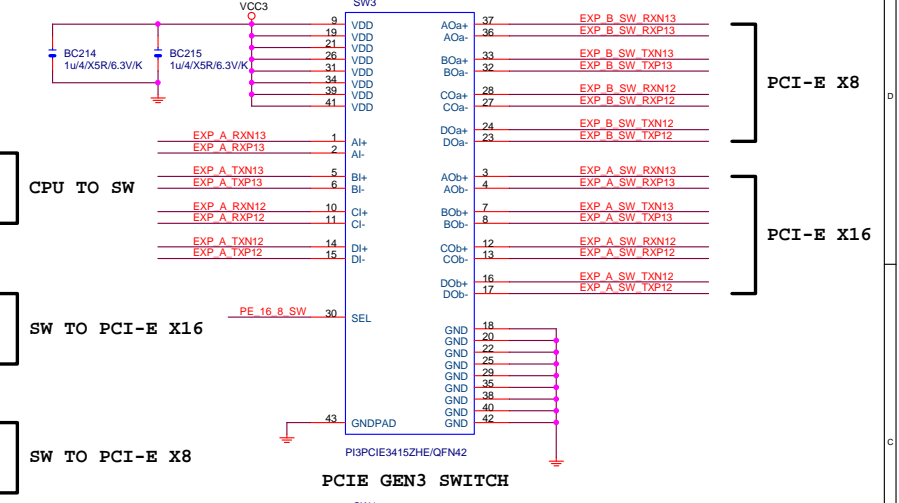
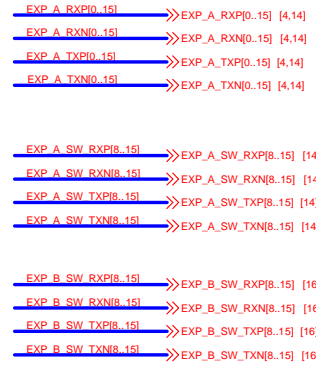
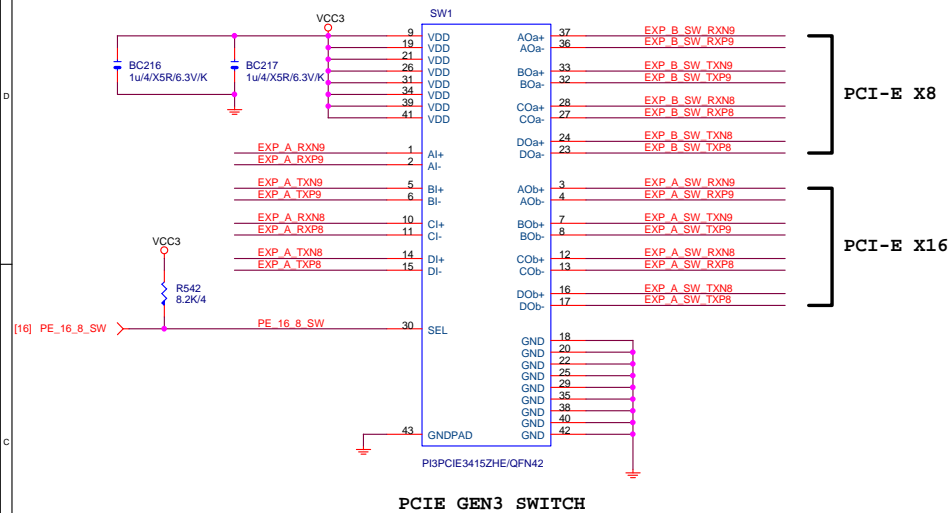
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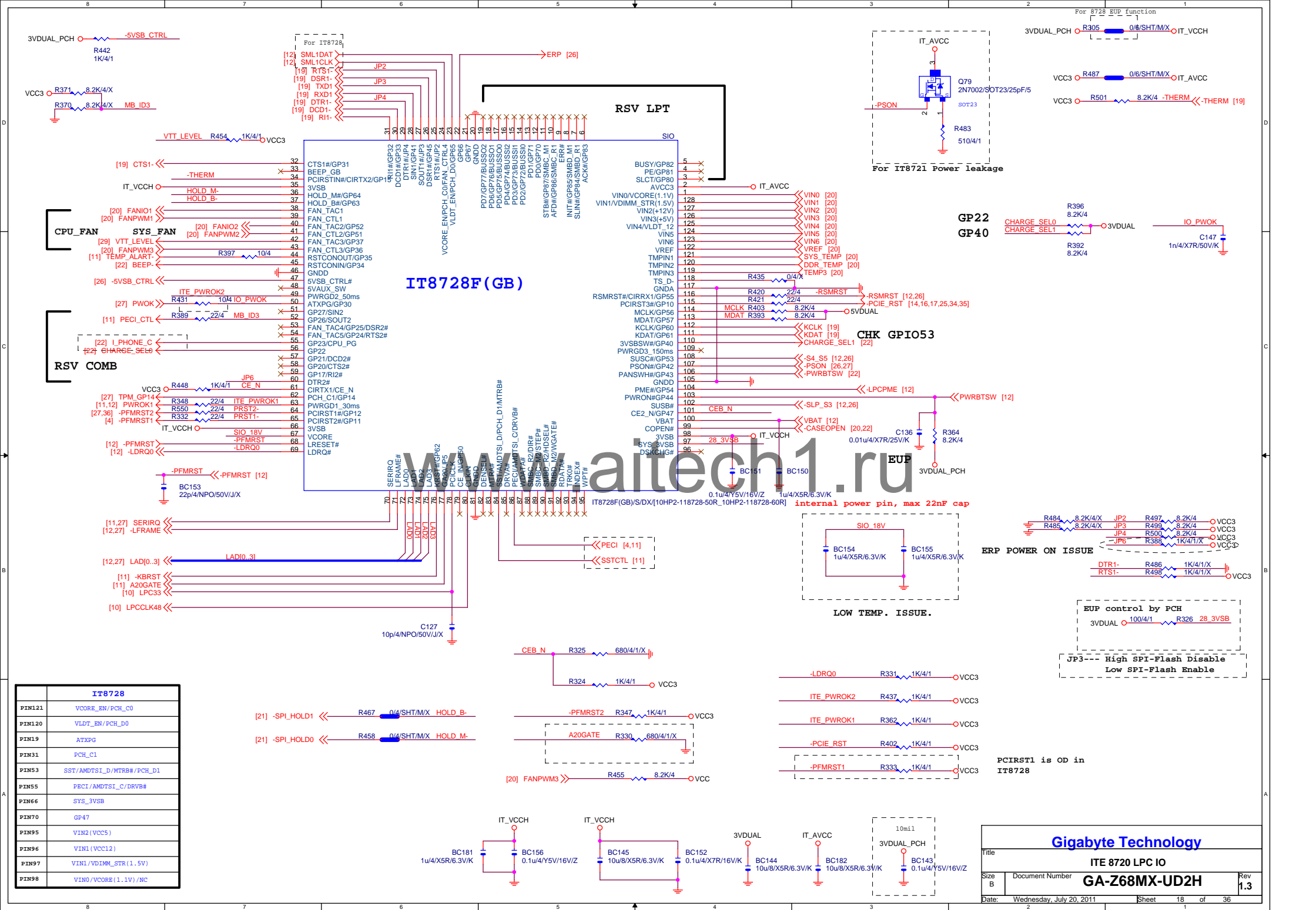


Function	SEL
xI--> x0a	L
xI--> x0b	H

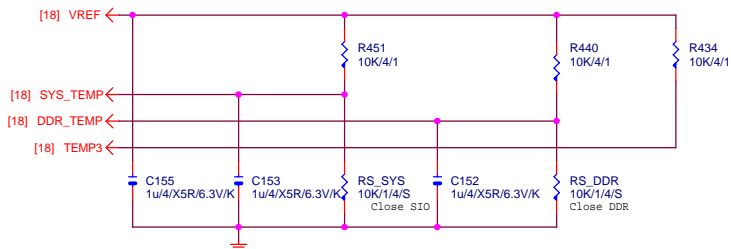




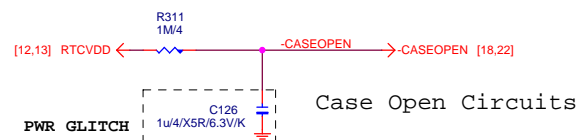
			
PCI EXPRESS X 8 PORT			
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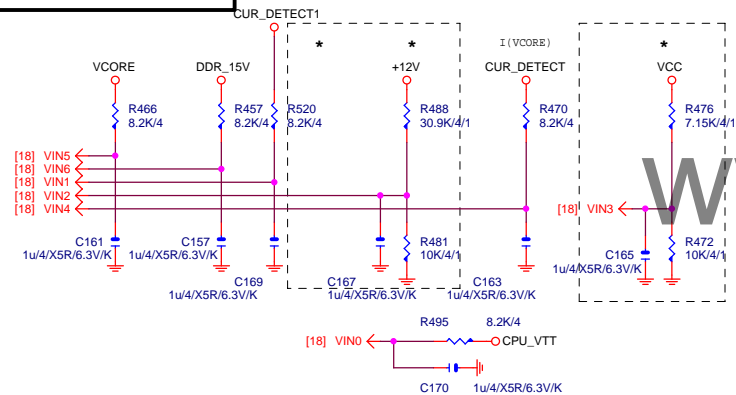
TEMP H/W MONITOR



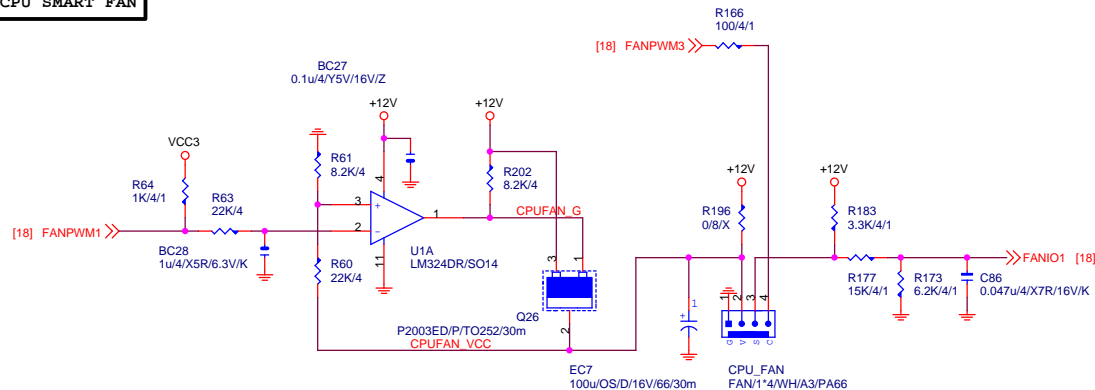
CASE OPEN



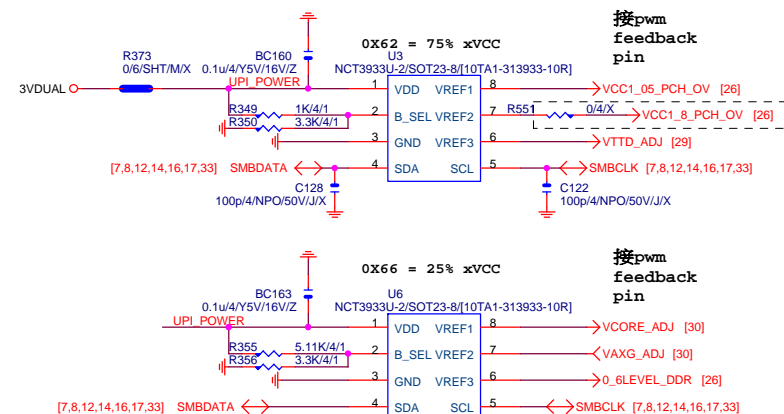
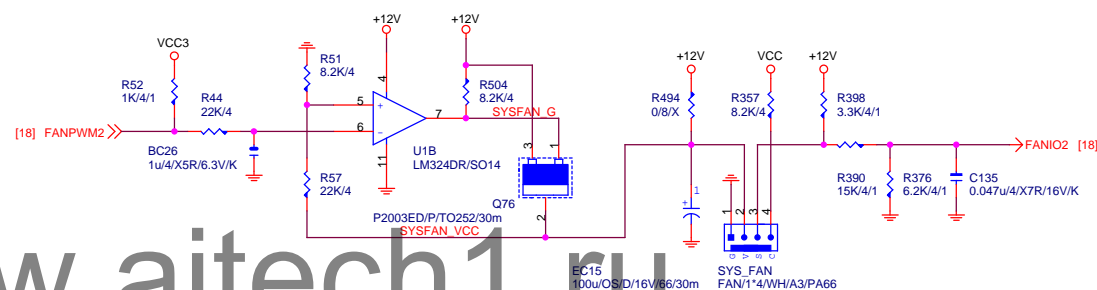
VOLTAGE-- H/W MONITOR



CPU SMART FAN



SYS SMART FAN



DUAL BIOS

The diagram illustrates a Dual BIOS system with two BIOS chips, M_BIOS and B_BIOS, connected to a motherboard. Both chips are 32M/SPI/SO8/200mil/S.

M_BIOS Connections:

- Pin 1 (CS#): -ICH_SPI_CS (via R299, 22/4)
- Pin 2 (SO): SPI_MISO
- Pin 3 (WP#): -SPI_WP0
- Pin 4 (VSS): Ground
- Pin 8 (VDD): VCC3 (via R297, 0/4/SHT/M/X)
- Pin 7 (HOLD#): -SPI_HOLD0 (via BC142, 0.1u/4/Y5V/16V/Z)
- Pin 6 (SCK): ICH_SPI_CLK
- Pin 5 (SI): ICH_SPI_MOSI (via C110, 10p/4/NPO/50V/J/X)

B_BIOS Connections:

- Pin 1 (CS#): -ICH_SPI_CS (via R300, 22/4)
- Pin 2 (SO): SPI_MISO
- Pin 3 (WP#): -SPI_WP1
- Pin 4 (VSS): Ground
- Pin 8 (VDD): VCC3 (via R282, 0/4/SHT/M/X)
- Pin 7 (HOLD#): -SPI_HOLD1 (via BC140, 0.1u/4/Y5V/16V/Z)
- Pin 6 (SCK): ICH_SPI_CLK
- Pin 5 (SI): ICH_SPI_MOSI

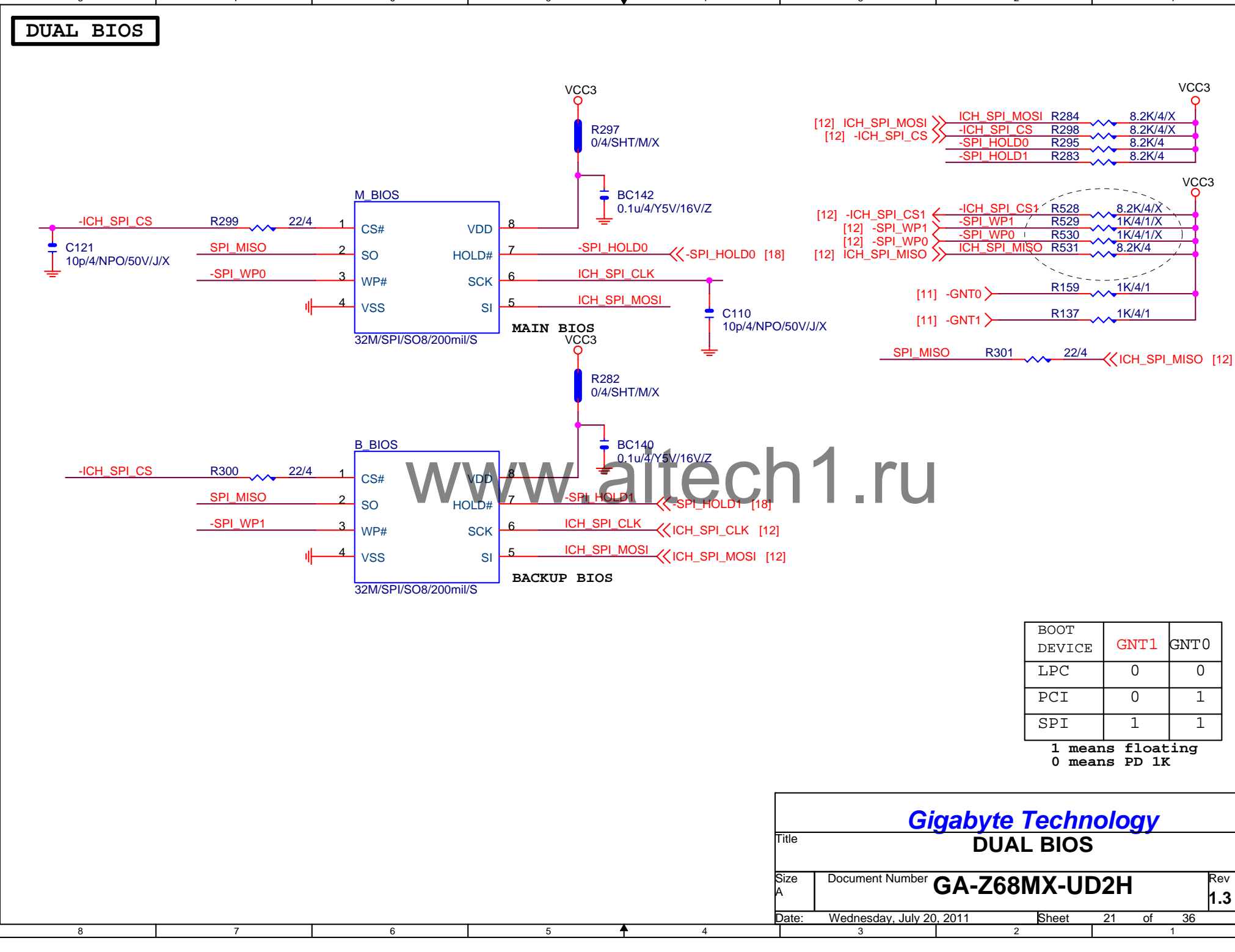
Other Connections:

- Pin 12 of ICH_SPI_MOSI: ICH_SPI_MOSI (via R284, 8.2K/4/X)
- Pin 12 of -ICH_SPI_CS: -ICH_SPI_CS (via R298, 8.2K/4/X)
- Pin 12 of -SPI_HOLD0: -SPI_HOLD0 (via R295, 8.2K/4)
- Pin 12 of -SPI_HOLD1: -SPI_HOLD1 (via R283, 8.2K/4)
- Pin 12 of -ICH_SPI_CS1: -ICH_SPI_CS1 (via R528, 8.2K/4/X)
- Pin 12 of -SPI_WP1: -SPI_WP1 (via R529, 1K/4/1/X)
- Pin 12 of -SPI_WP0: -SPI_WP0 (via R530, 1K/4/1/X)
- Pin 12 of ICH_SPI_MISO: ICH_SPI_MISO (via R531, 8.2K/4)
- Pin 11 of -GNT0: -GNT0 (via R159, 1K/4/1)
- Pin 11 of -GNT1: -GNT1 (via R137, 1K/4/1)
- Pin 12 of SPI_MISO: SPI_MISO (via R301, 22/4)

BIOS Configuration Table:

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K



DUAL BIOS

The diagram illustrates a Dual BIOS configuration using two 32M/SPI/SO8/200mil/S chips: **M BIOS** and **B BIOS**.

Main BIOS (M BIOS) Connections:

- Pin 1 (CS#): -ICH_SPI_CS (pull-up R299, 22/4)
- Pin 2 (SO): SPI_MISO
- Pin 3 (WP#): -SPI_WP0
- Pin 4 (VSS): Ground
- Pin 8 (VDD): VCC3 (pull-down R297, 0/4/SHT/M/X)
- Pin 7 (HOLD#): -SPI_HOLD0 (pull-down BC142, 0.1u/4/Y5V/16V/Z)
- Pin 6 (SCK): ICH_SPI_CLK
- Pin 5 (SI): ICH_SPI_MOSI (pull-down C110, 10p/4/NPO/50V/J/X)

Backup BIOS (B BIOS) Connections:

- Pin 1 (CS#): -ICH_SPI_CS (pull-up R300, 22/4)
- Pin 2 (SO): SPI_MISO
- Pin 3 (WP#): -SPI_WP1
- Pin 4 (VSS): Ground
- Pin 8 (VDD): VCC3 (pull-down R282, 0/4/SHT/M/X)
- Pin 7 (HOLD#): -SPI_HOLD1 (pull-down BC140, 0.1u/4/Y5V/16V/Z)
- Pin 6 (SCK): ICH_SPI_CLK
- Pin 5 (SI): ICH_SPI_MOSI

Signal Connections:

- [12] ICH_SPI_MOSI <-> ICH_SPI_MOSI (R284, 8.2K/4/X)
- [12] -ICH_SPI_CS <-> -ICH_SPI_CS (R298, 8.2K/4/X)
- SPI_HOLD0 <-> -SPI_HOLD0 [18]
- [12] -ICH_SPI_CS1 <-> -ICH_SPI_CS1 (R528, 8.2K/4/X)
- [12] -SPI_WP1 <-> -SPI_WP1 (R529, 1K/4/1/X)
- [12] -SPI_WP0 <-> -SPI_WP0 (R530, 1K/4/1/X)
- [12] ICH_SPI_MISO <-> ICH_SPI_MISO (R531, 8.2K/4)
- [11] -GNT0 <-> -GNT0 (R159, 1K/4/1)
- [11] -GNT1 <-> -GNT1 (R137, 1K/4/1)
- SPI_MISO <-> ICH_SPI_MISO [12] (R301, 22/4)

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BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

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DUAL BIOS

The diagram illustrates a Dual BIOS configuration for a motherboard. It features two BIOS chips: **MAIN BIOS** and **BACKUP BIOS**, both 32M/SPI/SO8/200mil/S.

MAIN BIOS Connections:

- CS#:** Connected to **-ICH_SPI_CS** via resistor R299 (22/4).
- SO:** Connected to **SPI_MISO**.
- WP#:** Connected to **-SPI_WP0**.
- VSS:** Grounded.
- VDD:** Connected to **VCC3** via resistor R297 (0/4/SHT/M/X) and capacitor BC142 (0.1u/4/Y5V/16V/Z).
- HOLD#:** Connected to **-SPI_HOLD0** (pin 18).
- SCK:** Connected to **ICH_SPI_CLK**.
- SI:** Connected to **ICH_SPI_MOSI** via capacitor C110 (10p/4/NPO/50V/J/X).

BACKUP BIOS Connections:

- CS#:** Connected to **-ICH_SPI_CS** via resistor R300 (22/4).
- SO:** Connected to **SPI_MISO**.
- WP#:** Connected to **-SPI_WP1**.
- VSS:** Grounded.
- VDD:** Connected to **VCC3** via resistor R282 (0/4/SHT/M/X) and capacitor BC140 (0.1u/4/Y5V/16V/Z).
- HOLD#:** Connected to **-SPI_HOLD1** (pin 18).
- SCK:** Connected to **ICH_SPI_CLK** (pin 12).
- SI:** Connected to **ICH_SPI_MOSI** (pin 12).

Other Connections:

- ICH_SPI_MOSI:** Connected to **ICH_SPI_MOSI** (pin 12) via resistor R284 (8.2K/4/X).
- ICH_SPI_CS:** Connected to **-ICH_SPI_CS** (pin 12) via resistor R298 (8.2K/4/X).
- SPI_HOLD0:** Connected to **-SPI_HOLD0** (pin 12) via resistor R295 (8.2K/4).
- SPI_HOLD1:** Connected to **-SPI_HOLD1** (pin 12) via resistor R283 (8.2K/4).
- ICH_SPI_CS1:** Connected to **-ICH_SPI_CS1** (pin 12) via resistor R528 (8.2K/4/X).
- SPI_WP1:** Connected to **-SPI_WP1** (pin 12) via resistor R529 (1K/4/1/X).
- SPI_WP0:** Connected to **-SPI_WP0** (pin 12) via resistor R530 (1K/4/1/X).
- ICH_SPI_MISO:** Connected to **ICH_SPI_MISO** (pin 12) via resistor R531 (8.2K/4).
- GNT0:** Connected to **-GNT0** (pin 11) via resistor R159 (1K/4/1).
- GNT1:** Connected to **-GNT1** (pin 11) via resistor R137 (1K/4/1).
- SPI_MISO:** Connected to **ICH_SPI_MISO** (pin 12) via resistor R301 (22/4).

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BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

Title

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DUAL BIOS

The diagram illustrates a Dual BIOS configuration for a motherboard. It features two BIOS chips: **MAIN BIOS** and **BACKUP BIOS**, both 32M/SPI/SO8/200mil/S.

MAIN BIOS Connections:

- CS#:** Connected to **-ICH_SPI_CS** via resistor R299 (22/4).
- SO:** Connected to **SPI_MISO**.
- WP#:** Connected to **-SPI_WP0**.
- VSS:** Grounded.
- VDD:** Connected to **VCC3** via resistor R297 (0/4/SHT/M/X) and capacitor BC142 (0.1u/4/Y5V/16V/Z).
- HOLD#:** Connected to **-SPI_HOLD0** (pin 18).
- SCK:** Connected to **ICH_SPI_CLK**.
- SI:** Connected to **ICH_SPI_MOSI** via capacitor C110 (10p/4/NPO/50V/J/X).

BACKUP BIOS Connections:

- CS#:** Connected to **-ICH_SPI_CS** via resistor R300 (22/4).
- SO:** Connected to **SPI_MISO**.
- WP#:** Connected to **-SPI_WP1**.
- VSS:** Grounded.
- VDD:** Connected to **VCC3** via resistor R282 (0/4/SHT/M/X) and capacitor BC140 (0.1u/4/Y5V/16V/Z).
- HOLD#:** Connected to **-SPI_HOLD1** (pin 18).
- SCK:** Connected to **ICH_SPI_CLK** (pin 12).
- SI:** Connected to **ICH_SPI_MOSI** (pin 12).

Other Connections:

- ICH_SPI_MOSI:** Connected to **ICH_SPI_MOSI** (pin 12) via resistor R284 (8.2K/4/X).
- ICH_SPI_CS:** Connected to **-ICH_SPI_CS** (pin 12) via resistor R298 (8.2K/4/X).
- SPI_HOLD0:** Connected to **-SPI_HOLD0** (pin 12) via resistor R295 (8.2K/4).
- SPI_HOLD1:** Connected to **-SPI_HOLD1** (pin 12) via resistor R283 (8.2K/4).
- ICH_SPI_CS1:** Connected to **-ICH_SPI_CS1** (pin 12) via resistor R528 (8.2K/4/X).
- SPI_WP1:** Connected to **-SPI_WP1** (pin 12) via resistor R529 (1K/4/1/X).
- SPI_WP0:** Connected to **-SPI_WP0** (pin 12) via resistor R530 (1K/4/1/X).
- ICH_SPI_MISO:** Connected to **ICH_SPI_MISO** (pin 12) via resistor R531 (8.2K/4).
- GNT0:** Connected to **-GNT0** (pin 11) via resistor R159 (1K/4/1).
- GNT1:** Connected to **-GNT1** (pin 11) via resistor R137 (1K/4/1).
- SPI_MISO:** Connected to **ICH_SPI_MISO** (pin 12) via resistor R301 (22/4).

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BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

Title

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DUAL BIOS

The diagram illustrates a Dual BIOS configuration for a motherboard. It features two BIOS chips: **MAIN BIOS** and **BACKUP BIOS**, both labeled **32M/SPI/SO8/200mil/S**.

MAIN BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R299** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP0**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R297** (0/4/SHT/M/X) and capacitor **BC142** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD0** (labeled **<<-SPI_HOLD0 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK**.
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** through capacitor **C110** (10p/4/NPO/50V/J/X).

BACKUP BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R300** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP1**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R282** (0/4/SHT/M/X) and capacitor **BC140** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD1** (labeled **<<-SPI_HOLD1 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK** (labeled **<<ICH_SPI_CLK [12]**).
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** (labeled **<<ICH_SPI_MOSI [12]**).

Peripheral Connections:

- ICH_SPI_MOSI [12]:** Connected to **ICH_SPI_MOSI** through resistor **R284** (8.2K/4/X).
- ICH_SPI_CS [12]:** Connected to **-ICH_SPI_CS** through resistor **R298** (8.2K/4/X).
- SPI_HOLD0 [12]:** Connected to **-SPI_HOLD0** through resistor **R295** (8.2K/4).
- SPI_HOLD1 [12]:** Connected to **-SPI_HOLD1** through resistor **R283** (8.2K/4).
- ICH_SPI_CS1 [12]:** Connected to **-ICH_SPI_CS1** through resistor **R528** (8.2K/4/X).
- SPI_WP1 [12]:** Connected to **-SPI_WP1** through resistor **R529** (1K/4/1/X).
- SPI_WP0 [12]:** Connected to **-SPI_WP0** through resistor **R530** (1K/4/1/X).
- ICH_SPI_MISO [12]:** Connected to **ICH_SPI_MISO** through resistor **R531** (8.2K/4).
- GNT0 [11]:** Connected to **-GNT0** through resistor **R159** (1K/4/1).
- GNT1 [11]:** Connected to **-GNT1** through resistor **R137** (1K/4/1).
- SPI_MISO:** Connected to **ICH_SPI_MISO [12]** through resistor **R301** (22/4).

Legend:

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

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DUAL BIOS

The schematic shows two SPI chips, M_BIOS and B_BIOS, both labeled "32M/SPI/SO8/200mil/S".

- M_BIOS Connections:**
 - Pin 1 (CS#) to -ICH_SPI_CS via R299 (22/4).
 - Pin 2 (SO) to SPI_MISO.
 - Pin 3 (WP#) to -SPI_WP0.
 - Pin 4 (VSS) to ground.
 - Pin 8 (VDD) to VCC3 via R297 (0/4/SHT/M/X) and BC142 (0.1u/4/Y5V/16V/Z).
 - Pin 7 (HOLD#) to -SPI_HOLD0 <<-SPI_HOLD0 [18].
 - Pin 6 (SCK) to ICH_SPI_CLK.
 - Pin 5 (SI) to ICH_SPI_MOSI.
- B_BIOS Connections:**
 - Pin 1 (CS#) to -ICH_SPI_CS via R300 (22/4).
 - Pin 2 (SO) to SPI_MISO.
 - Pin 3 (WP#) to -SPI_WP1.
 - Pin 4 (VSS) to ground.
 - Pin 8 (VDD) to VCC3 via R282 (0/4/SHT/M/X) and BC140 (0.1u/4/Y5V/16V/Z).
 - Pin 7 (HOLD#) to -SPI_HOLD1 <<-SPI_HOLD1 [18].
 - Pin 6 (SCK) to ICH_SPI_CLK << ICH_SPI_CLK [12].
 - Pin 5 (SI) to ICH_SPI_MOSI << ICH_SPI_MOSI [12].
- Other Components:**
 - C121 (10p/4/NPO/50V/J/X) at pin 1 of M_BIOS.
 - C110 (10p/4/NPO/50V/J/X) at pin 5 of M_BIOS.
 - R284, R298, R295, R283 (8.2K/4/X, 8.2K/4/X, 8.2K/4, 8.2K/4) connecting ICH_SPI signals to VCC3.
 - R528, R529, R530, R531 (8.2K/4/X, 1K/4/1/X, 1K/4/1/X, 8.2K/4) connecting -ICH_SPI signals to VCC3.
 - R159, R137 (1K/4/1) connecting -GNT0, -GNT1 to VCC3.
 - R301 (22/4) connecting SPI_MISO to ICH_SPI_MISO [12].

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BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

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DUAL BIOS

M BIOS

32M/SPI/SO8/200mil/S

MAIN BIOS

VCC3

B BIOS

32M/SPI/SO8/200mil/S

BACKUP BIOS

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BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology

DUAL BIOS

Title

Size A Document Number **GA-Z68MX-UD2H** Rev **1.3**

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DUAL BIOS

M BIOS

32M/SPI/SO8/200mil/S

MAIN BIOS

VCC3

B BIOS

32M/SPI/SO8/200mil/S

BACKUP BIOS

www.aitech1.ru

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology

DUAL BIOS

Title

Size A Document Number **GA-Z68MX-UD2H** Rev **1.3**

Date: Wednesday, July 20, 2011 Sheet 21 of 36

DUAL BIOS

The diagram illustrates a Dual BIOS configuration for a motherboard. It features two BIOS chips: the **MAIN BIOS** (top) and the **BACKUP BIOS** (bottom), both labeled **32M/SPI/SO8/200mil/S**.

Main BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R299** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP0**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R297** (0/4/SHT/M/X) and capacitor **BC142** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD0** (labeled **<<-SPI_HOLD0 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK**.
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** through capacitor **C110** (10p/4/NPO/50V/J/X).

Backup BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R300** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP1**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R282** (0/4/SHT/M/X) and capacitor **BC140** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD1** (labeled **<<-SPI_HOLD1 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK** (labeled **<<ICH_SPI_CLK [12]**).
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** (labeled **<<ICH_SPI_MOSI [12]**).

Peripheral Connections:

- ICH_SPI_MOSI:** Connected to **ICH_SPI_MOSI** through resistor **R284** (8.2K/4/X).
- ICH_SPI_CS:** Connected to **ICH_SPI_CS** through resistor **R298** (8.2K/4/X).
- SPI_HOLD0:** Connected to **SPI_HOLD0** through resistor **R295** (8.2K/4).
- SPI_HOLD1:** Connected to **SPI_HOLD1** through resistor **R283** (8.2K/4).
- SPI_WP1:** Connected to **SPI_WP1** through resistor **R528** (8.2K/4/X).
- SPI_WP0:** Connected to **SPI_WP0** through resistor **R529** (1K/4/1/X).
- SPI_MISO:** Connected to **SPI_MISO** through resistor **R530** (1K/4/1/X).
- SPI_MISO:** Connected to **SPI_MISO** through resistor **R531** (8.2K/4).
- GNT0:** Connected to **GNT0** through resistor **R159** (1K/4/1).
- GNT1:** Connected to **GNT1** through resistor **R137** (1K/4/1).
- SPI_MISO:** Connected to **SPI_MISO** through resistor **R301** (22/4).

Table 1: BOOT DEVICE

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

Title

Size A Document Number **GA-Z68MX-UD2H** Rev **1.3**

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DUAL BIOS

The diagram illustrates the Dual BIOS circuit for the GA-Z68MX-UD2H motherboard. It features two BIOS chips, M_BIOS and B_BIOS, both 32M/SPI/SO8/200mil/S. The M_BIOS chip is connected to VCC3, VDD, HOLD#, SCK, SI, CS#, SO, WP#, and VSS. The B_BIOS chip is connected to VCC3, VDD, HOLD#, SCK, SI, CS#, SO, WP#, and VSS. The circuit includes resistors (R297, R298, R299, R283, R284, R528, R529, R530, R531, R159, R137, R301, R300), capacitors (C121, C110, BC142, BC140), and a watermark 'www.aitech1.ru'.

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology		
DUAL BIOS		
Title	Document Number	
Size A	GA-Z68MX-UD2H	
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DUAL BIOS

The diagram illustrates a Dual BIOS configuration for a motherboard. It features two BIOS chips: **MAIN BIOS** and **BACKUP BIOS**, both labeled **32M/SPI/SO8/200mil/S**.

MAIN BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R299** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP0**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R297** (0/4/SHT/M/X) and capacitor **BC142** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD0** (labeled **<<-SPI_HOLD0 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK**.
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** through capacitor **C110** (10p/4/NPO/50V/J/X).

BACKUP BIOS Connections:

- Pin 1 (CS#):** Connected to **-ICH_SPI_CS** through resistor **R300** (22/4).
- Pin 2 (SO):** Connected to **SPI_MISO**.
- Pin 3 (WP#):** Connected to **-SPI_WP1**.
- Pin 4 (VSS):** Grounded.
- Pin 8 (VDD):** Connected to **VCC3** through resistor **R282** (0/4/SHT/M/X) and capacitor **BC140** (0.1u/4/Y5V/16V/Z).
- Pin 7 (HOLD#):** Connected to **-SPI_HOLD1** (labeled **<<-SPI_HOLD1 [18]**).
- Pin 6 (SCK):** Connected to **ICH_SPI_CLK** (labeled **<<ICH_SPI_CLK [12]**).
- Pin 5 (SI):** Connected to **ICH_SPI_MOSI** (labeled **<<ICH_SPI_MOSI [12]**).

Peripheral Connections:

- ICH_SPI_MOSI [12]:** Connected to **ICH_SPI_MOSI** through resistor **R284** (8.2K/4/X).
- ICH_SPI_CS [12]:** Connected to **-ICH_SPI_CS** through resistor **R298** (8.2K/4/X).
- SPI_HOLD0 [12]:** Connected to **-SPI_HOLD0** through resistor **R295** (8.2K/4).
- SPI_HOLD1 [12]:** Connected to **-SPI_HOLD1** through resistor **R283** (8.2K/4).
- ICH_SPI_CS1 [12]:** Connected to **-ICH_SPI_CS1** through resistor **R528** (8.2K/4/X).
- SPI_WP1 [12]:** Connected to **-SPI_WP1** through resistor **R529** (1K/4/1/X).
- SPI_WP0 [12]:** Connected to **-SPI_WP0** through resistor **R530** (1K/4/1/X).
- ICH_SPI_MISO [12]:** Connected to **ICH_SPI_MISO** through resistor **R531** (8.2K/4).
- GNT0 [11]:** Connected to **-GNT0** through resistor **R159** (1K/4/1).
- GNT1 [11]:** Connected to **-GNT1** through resistor **R137** (1K/4/1).
- SPI_MISO:** Connected to **ICH_SPI_MISO [12]** through resistor **R301** (22/4).

Legend:

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

Gigabyte Technology
DUAL BIOS

Title: **DUAL BIOS**

Size A: **GA-Z68MX-UD2H**

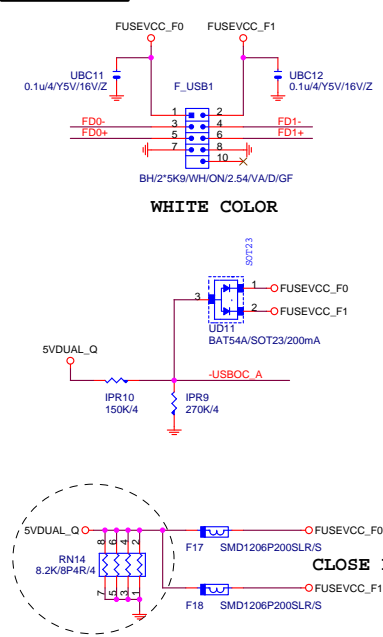
Document Number: **GA-Z68MX-UD2H**

Date: Wednesday, July 20, 2011

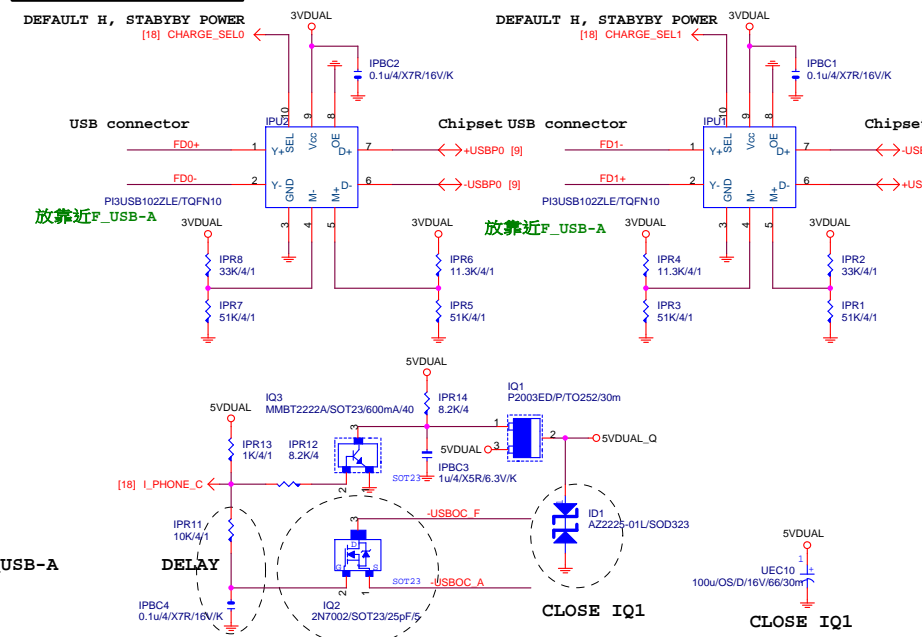
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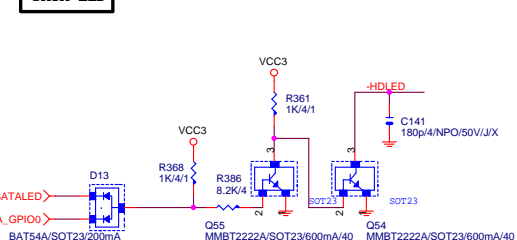
FRONT USB1



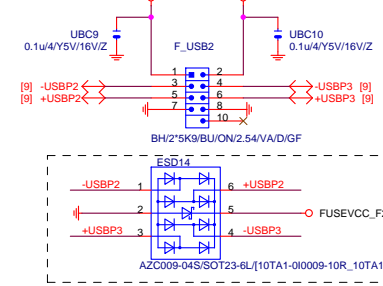
i_phone charger circuit



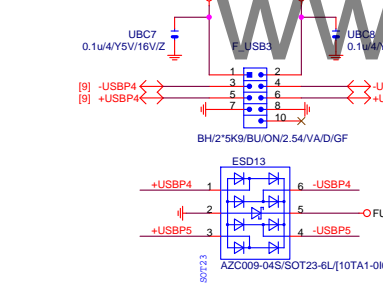
SATA LED



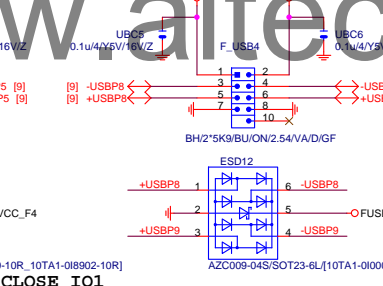
FRONT USB2



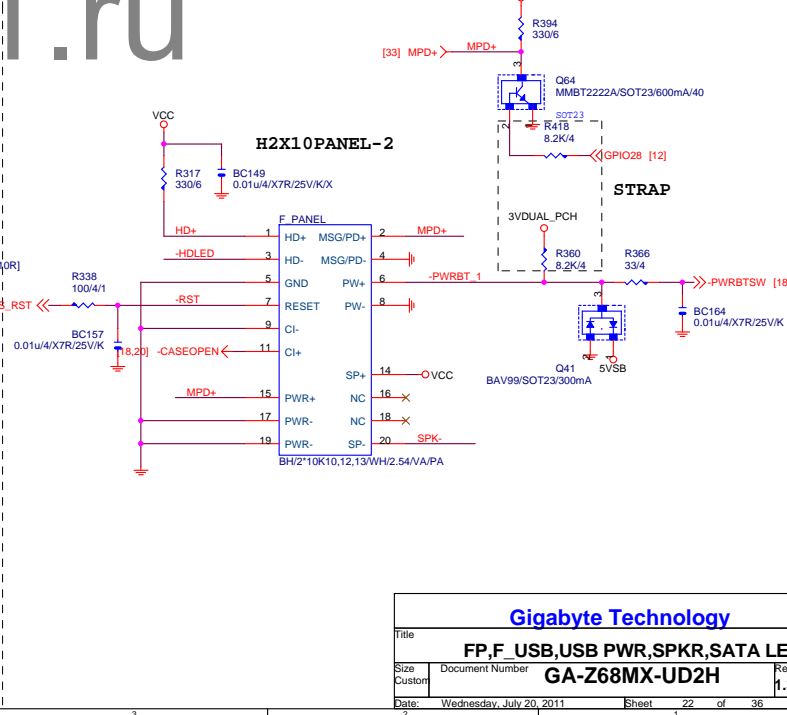
FRONT USB3



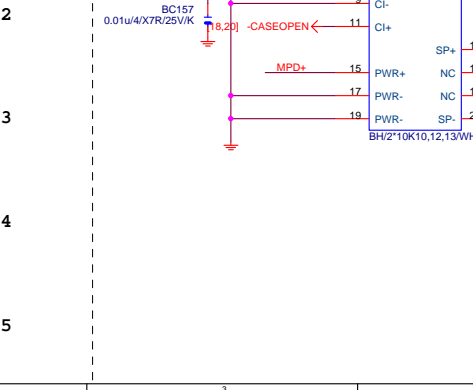
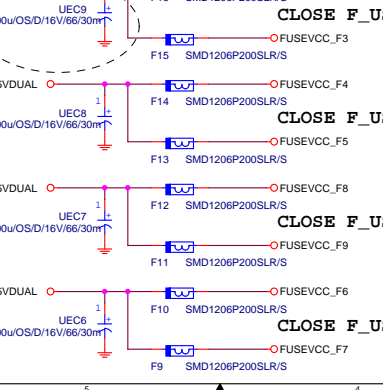
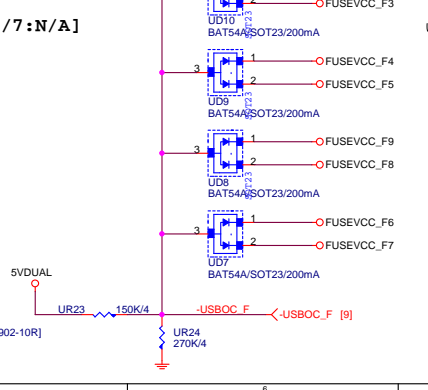
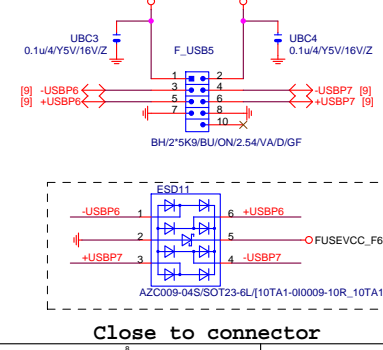
FRONT USB4



INTEL FRONT PANEL



FRONT USB5



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Title	FP,F_USB,USB PWR,SPKR,SATA LED	
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[24] CEN ←

[24] LFE ←

[24] S_SURR_L ←

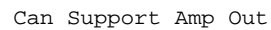
[24] S_SURR_R ←

CR59 8.2K/4/X



Analog Area

Can Support Amp Out



[illegible]

HDMI SPDIF

CR52
10/4

[23] SPDIFO2_HDMI

SPDIFO_HDMI

For HDMI SPDIF

CBC31
100pF/4NPO/50V/J

PIN

SPDIF_O
PH/1'2/BK/2.54/VA/D

For HDMI SPDIF

FUSEVCC_R

[23] SPDIF

G3 G1 G4 G2

DP_HDMI_SPDIFC

DP+HDMI+SPDIF/20P+19P+3P/BK/RA :: Location_DP_HDMI_SPDIF

The diagram shows a 6-pin connector labeled "AZALIA JACK". The pins are arranged in a 2x3 grid. The top row contains an orange pin, a cyan pin, and a black pin. The bottom row contains a black pin, a green pin, and a pink pin. Below the connector, a detailed wiring diagram shows the connections for each pin. The pins are labeled as follows:

- Pin 1 (Orange):** LINE1_JD (Left channel line-in)
- Pin 2 (Cyan):** AJ_A5 (Left channel ground)
- Pin 3 (Black):** FRONT_JD (Front channel line-in)
- Pin 4 (Black):** AJ_B5 (Front channel ground)
- Pin 5 (Green):** MIC1_JD (Microphone line-in)
- Pin 6 (Pink):** AJ_C5 (Microphone ground)

The wiring diagram also shows the connections for the other pins (A1, A2, B1, B2, C1, C2) and the ground connections (GND). The pins are color-coded to match the connector: BLUE for LINE-IN, GREEN for LINE-OUT, and PINK for MIC-IN.

LINE-OUT

[23] LINE_O_R

CEC6 100uF/OS/D/16V/66/30m

CR33 62/4

[23] LINE_O_L

CEC2 100uF/OS/D/16V/66/30m

CR11 62/4

CR10 10K/4/1

CR34 10K/4/1

AJ_B5

AJ_B2

CBC12 180pF/4/NPO/50V/J

CBC18 180pF/4/NPO/50V/J

Only reserved for AL888

LINE-IN

[23] LINE_IN_R

CR17 62/4

[23] LINE_IN_L

CR18 62/4

CR3 8.2K/4

CR4 8.2K/4

AJ_A5

AJ_A2

CBC13 180pF/4/NPO/50V/J

CBC10 180pF/4/NPO/50V/J

For 889A/888

BAT54A/SOT23/200mA

Verify MIC function in LINE-in

Verify MIC function in LINE-in

For 889A/888

BAT54A/SOT23/200mA

CR17 62/4

CR18 62/4

CR3 8.2K/4

CR4 8.2K/4

CBC13 180pF/NPO/50V/J

CBC10 180pF/NPO/50V/J

AJ_A5

AJ_A2

CO1

[23] LINE_IN_R

[23] LINE_IN_L

[23] VOCR

[23] MIC1_R ← CR13 62/4

[23] MIC1_L ← CR14 62/4

[23] MIC1_VREFO_L

[23] MIC1_VREFO_R

180pF 4/NPO/50V/J

CBC3

CBC2

180pF 4/NPO/50V/J

AJ_C5

AJ_C2

SURROUND

CEC9 100uOS/D/16V/66/30m
CEC5 100uOS/D/16V/66/30m

[23] Surr_R
[23] Surr_L

EMI

CR41 62/4
CR35 62/4

CR42 10K/4/1

BJ C5
BJC2

CBC19 180p/4/NPO/50V/J
CBC22 180p/4/NPO/50V/J

CR36 10K/4/1

[illegible]

SURR BACK

EMI

CEC1 100u/OS/D/16V/66/30m CR15 62/4

CEC3 100u/OS/D/16V/66/30m CR16 62/4

[23] S_SURR_R ←

[23] S_SURR_L ←

CR1 10K/4/1

BJ_A5

BJ_A2

CBC1 180p/4/NPO/50V/J

CBC21 180p/4/NPO/50V/J

AZALIA FRONT PANEL

F_AUDIO_H

Digital Area

Gigabyte Technology

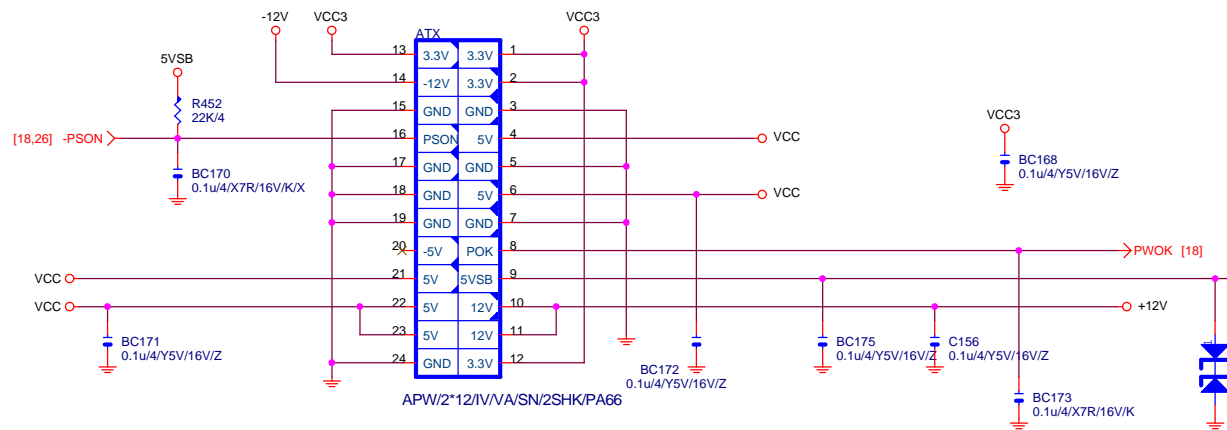
AUDIO JACK

GA-Z68MX-UD2H

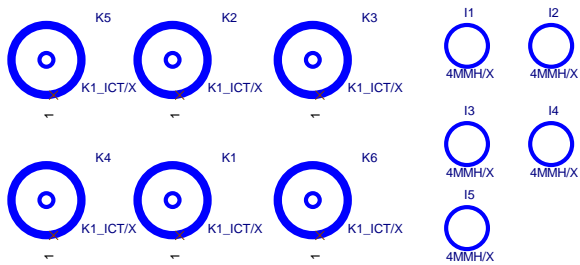
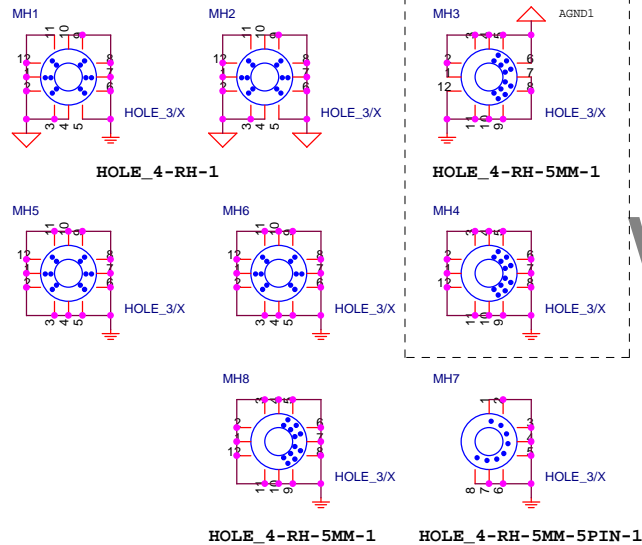
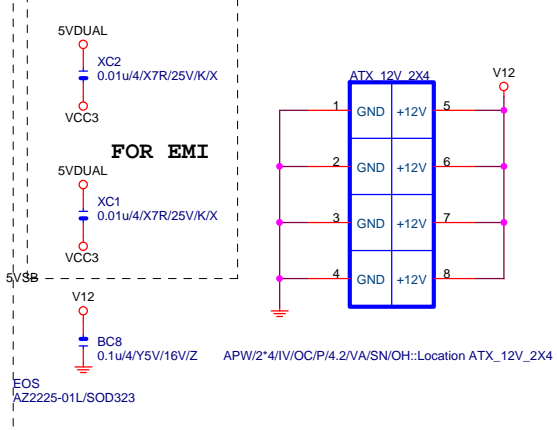
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ATXX24 POWER CONNECTOR

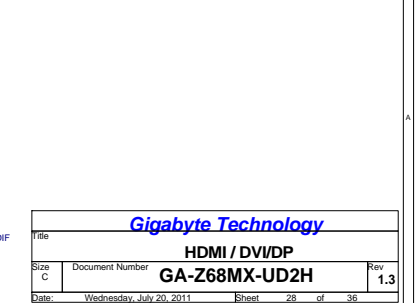
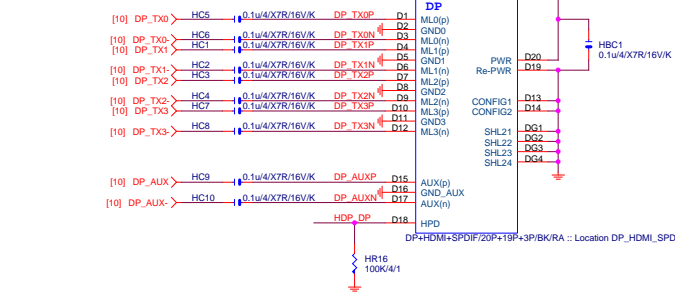
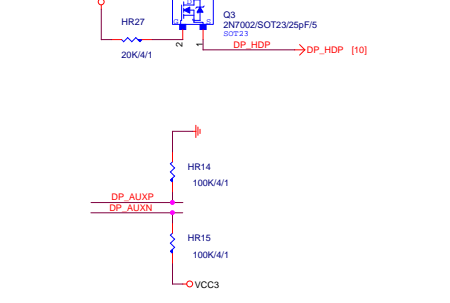
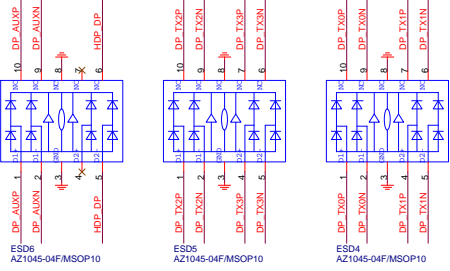
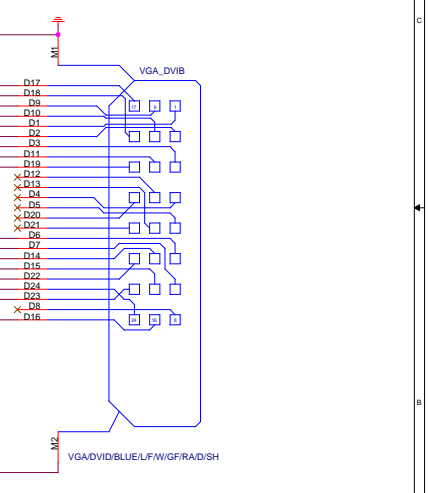
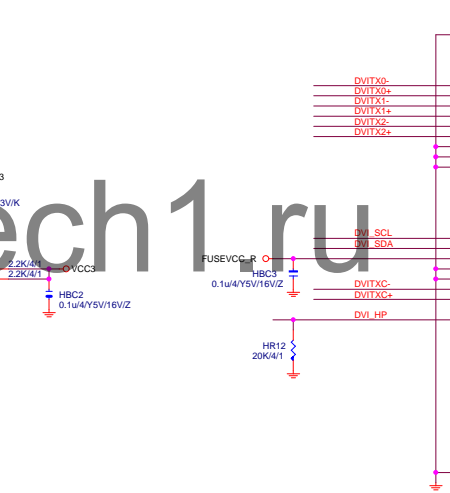
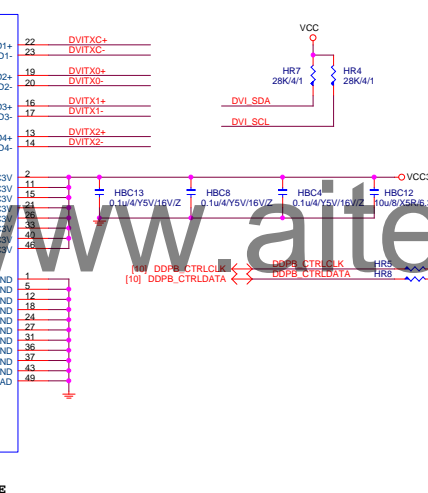
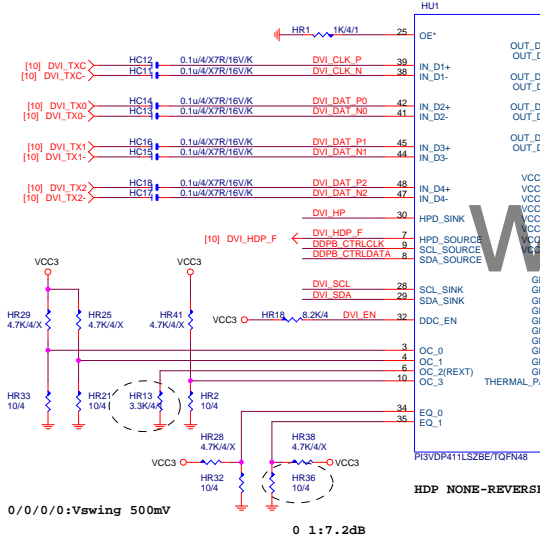
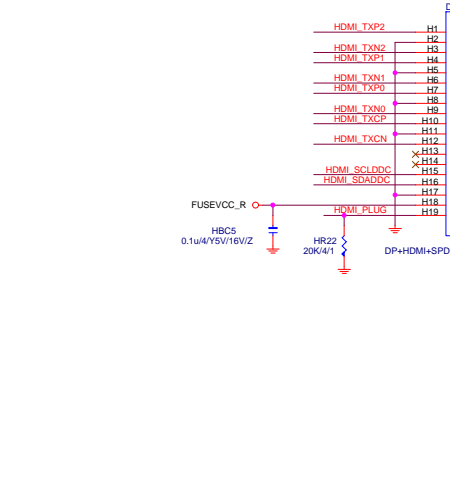
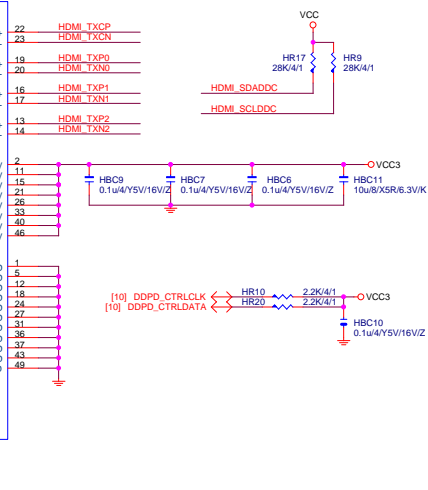
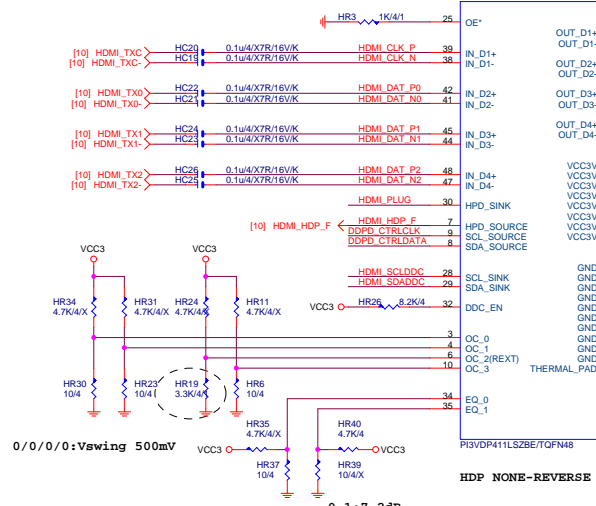


ATXX4 POWER CONNECTOR

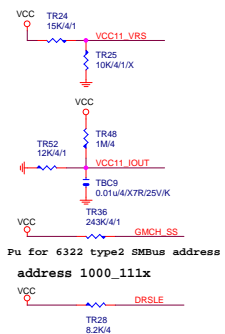


Gigabyte Technology

Title	ATX CONNECTOR		
Size	Document Number	GA-Z68MX-UD2H	Rev 1.3
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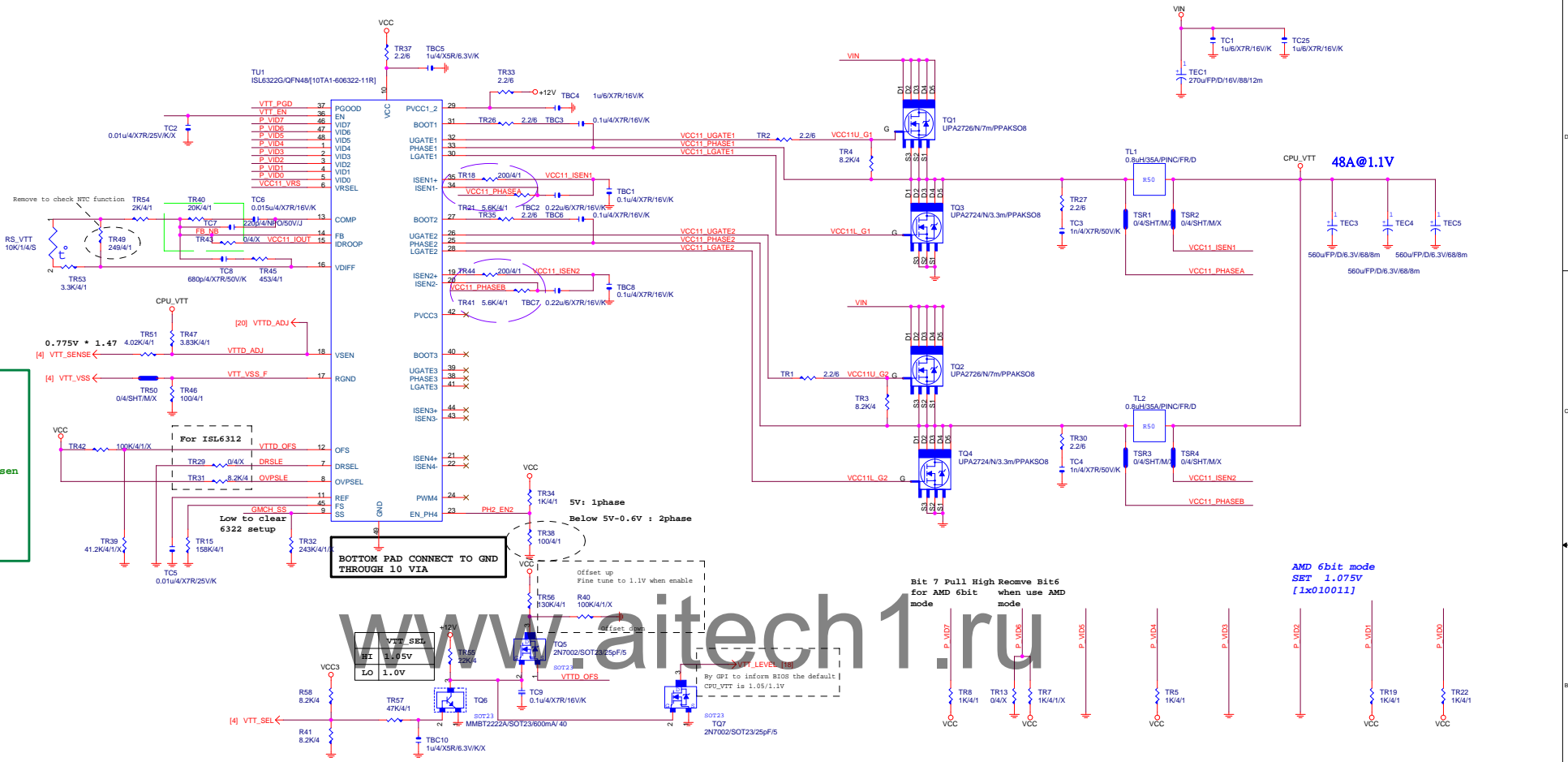

```
5V : AMD mode
0.6V~3V : VRD11 mode
0V : VRD10 mode
```



```

OCF貼做在146A
Isensx R270阻值設在590ohm
Iocpx=(IsensxRisensxPhase)/DCR
=[(120uAX590X2)/0.97m=146A
L/DCR=R*C
L=1uH DCR=0.97 mohm ,
1uH/0.97mohms=4.7XK0.22uF
Risens R260 阻值=4.7k ohm, Cisen
BC75=0.22u
Rt=10*{0.61-[1.035Xlog(FS)]}
Rt=R301=158 kohm , FS=170KHz
OVP=VDAC+225mV

```



VCCSA

PDG 0.8

	VSA_SEL
HI	0.85V
LO	0.925V

2.5LEVEL

VSA_REF

1u4/4X7R/6.3V/K

R31 10K/4/1

R33 5.23K/4/1

U1C LM324DR/SO14

Q13 UPA2725N/7m/PPAKS08

CPU_VTT

BC23 22u/8/XSR/6.3V/M

BC25 22u/8/XSR/6.3V/M

R45 100k/4/1

C44 1n4/X7R/50V/K

R38 40.2K/4/1

R50 8.2K/4/1

R36 2K/4/1

BC29 22u/8/XSR/6.3V/M

EC4 560u/FP/DIE.3V/68/8m

BC22 1u4/4X7R/6.3V/K

R37 0.1u4/X7R/25V/K/X

BC24 0.01u4/X7R/25V/K/X

[4] VSA_SENSE

VCCSA_PWR_SBO

VCC3

VTT_PGD

R24 1K/4/1

R28 8.2K/4/1

C18 0.1u4/X7R/16V/K/X

R27 22K/4/1

Q6 MMBT2222A/SOT23/600mA/40

Q7 2N7002/SOT23/25pF

C22 0.1u4/X7R/16V/K/X

Q8 2N7002/SOT23/25pF

Q9 1u4/X7R/16V/K/X

R32 63.4K/4/1

R46 22K/4/1

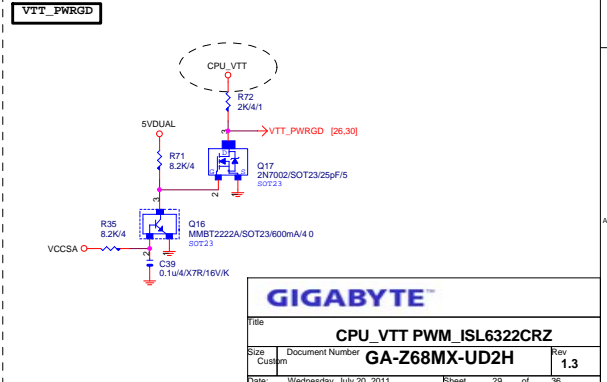
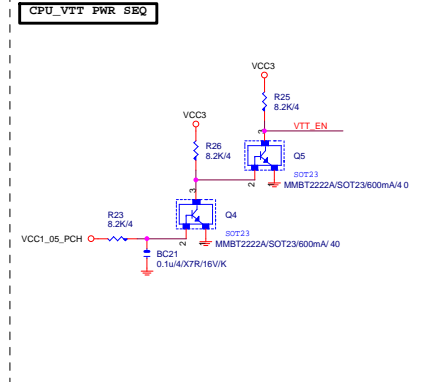
R39 1K/4/1

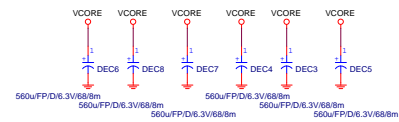
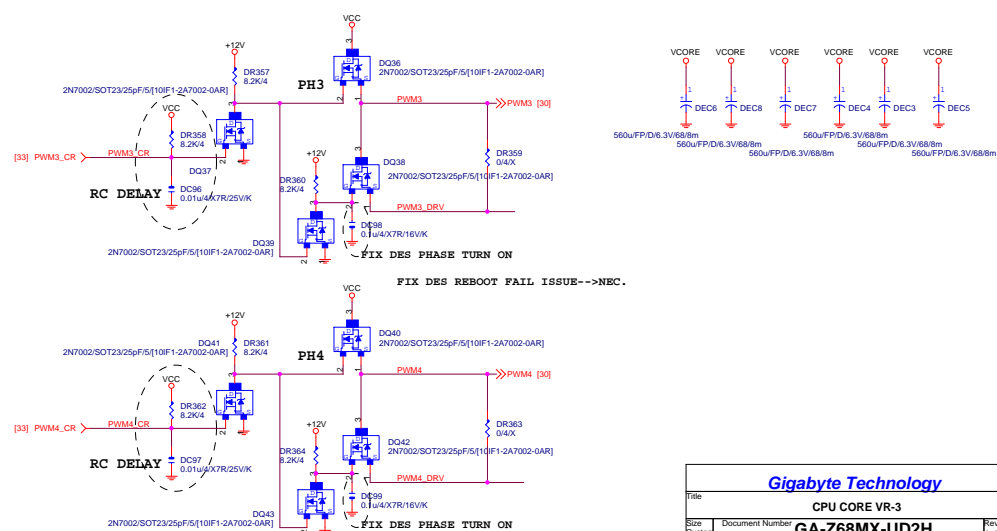
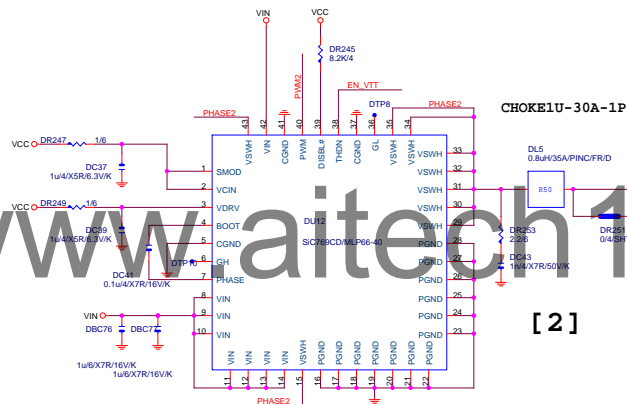
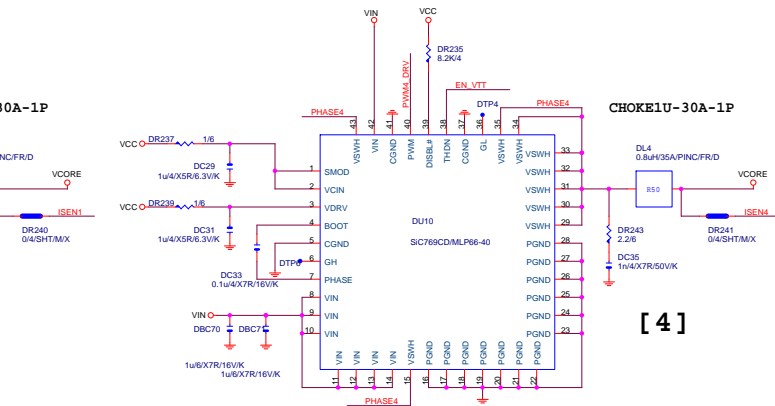
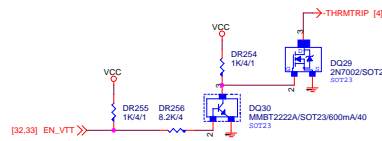
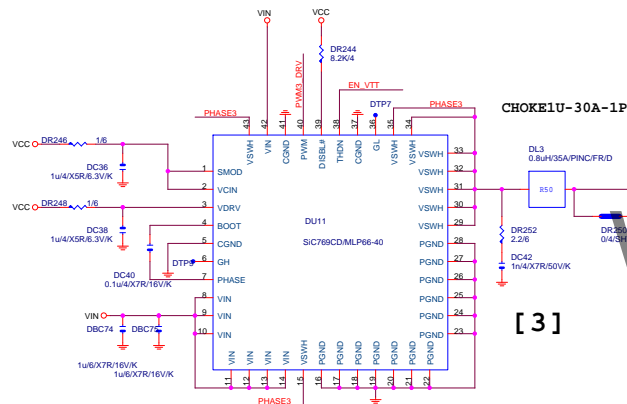
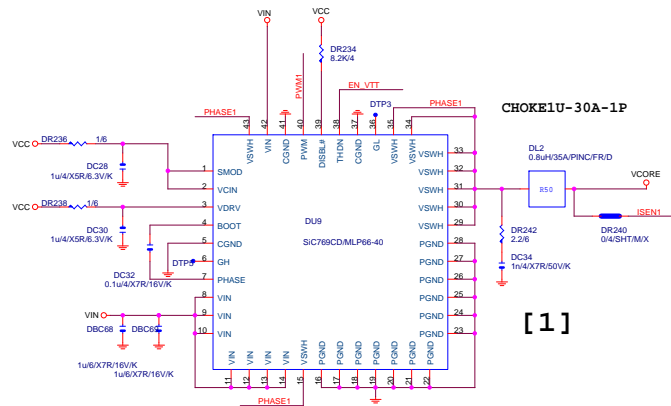
R47 100K/4/1

C45 0.1u4/X7R/16V/K/X

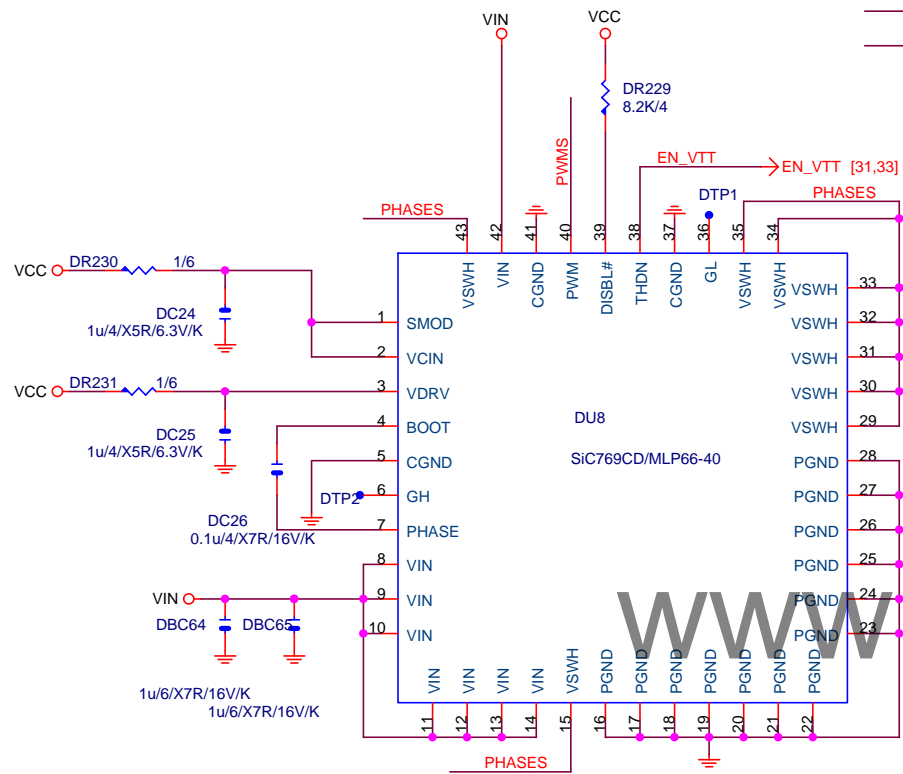
MMBT2222A/SOT23/600mA/40

[4] VSA_SEL





VAXG



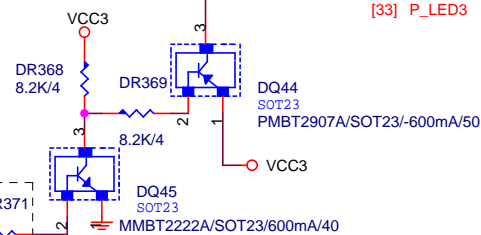
CHOK1U-30A-1P

DL6
0.8uH/35A/PINC/FR/D

DR233
2.2/6
DC27
1n4/X7R/50V/K

LED POWER

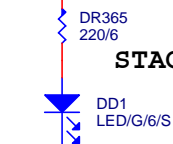
LED_PWR



PHASE LED

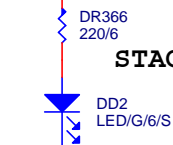
LED_PWR

STAGE1



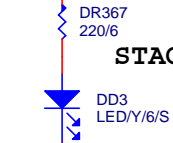
LED_PWR

STAGE2



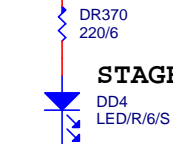
LED_PWR

STAGE3

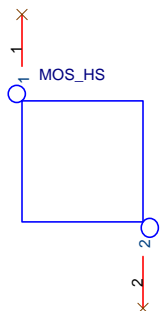


LED_PWR

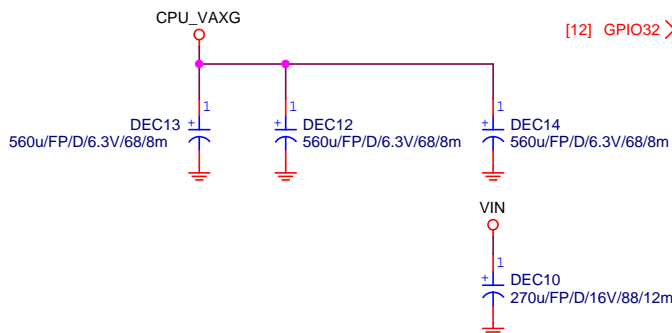
STAGE4



MOS HEATSINK



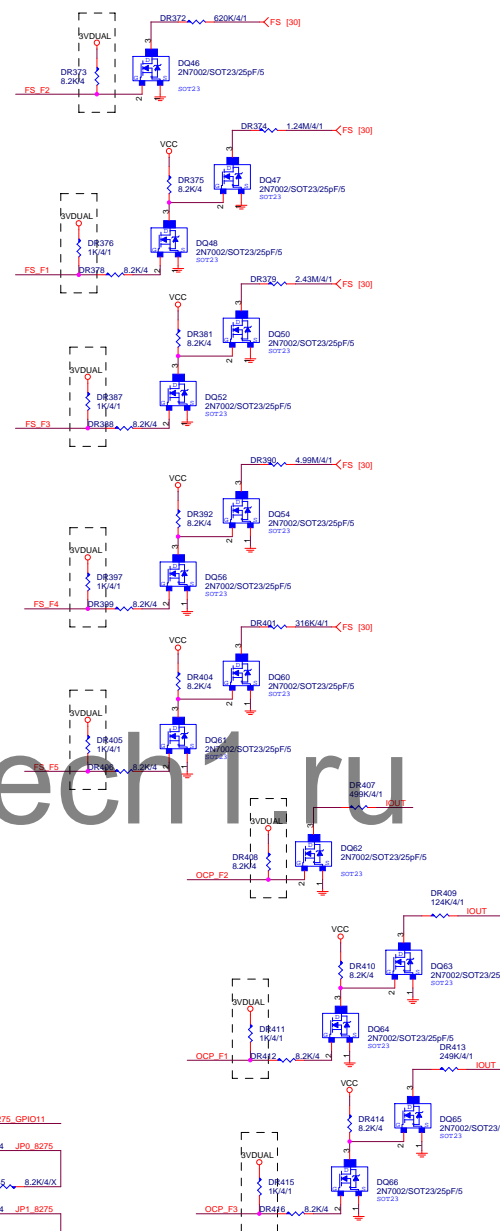
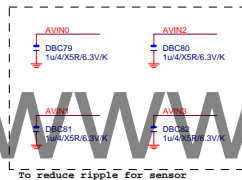
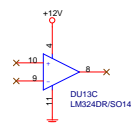
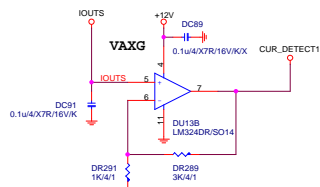
MOS HS/[12SP2-S06928-01R_12SP2-S06928-02R_12SP2-S06928-03R_12SP2-S06928-11R_12SP2-S06928-13R]



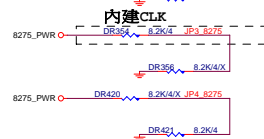
Gigabyte Technology

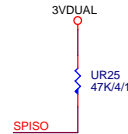
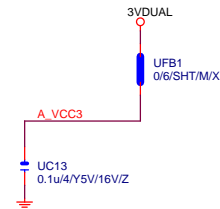
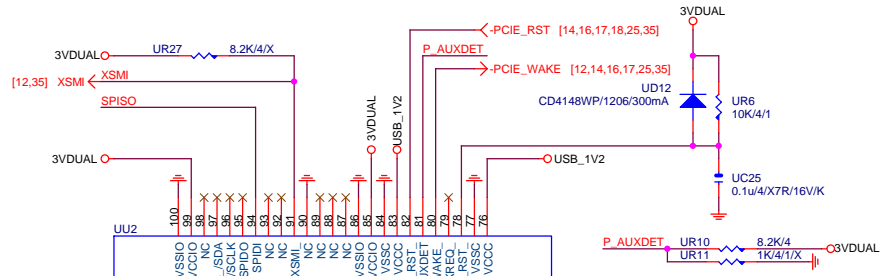
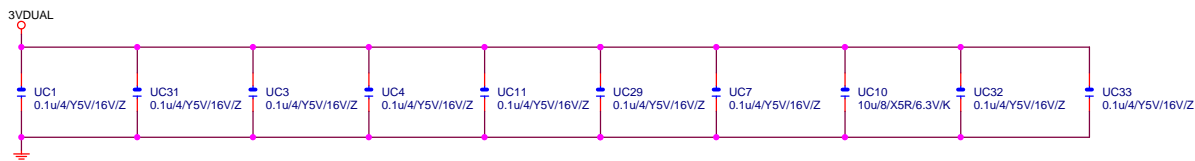
CPU CORE VR-2

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```
Pin24: GPIO4/JP0, LO : Indirect
mode:HI:bypass mode
Pin25: GPIO5/JP1, HI: Intel SVID mode
Pin26: GPIO6/JP2/B_LED1, Vcore detect LO: Disable
Pin27: GPIO7/JP3/B_LED1, 目前使用LO: External
clock source:HI FOR INTERNAL
Pin31: GPIO23/JP4/WM_DET, HI: Capture
mode:LO:Normal (Bypass mode)
Pin12: ASEL, HI: 4Eh.
```





SPIIM: Low=>SPI Rom.

UR9 8.2K/4

3VDUAL

USB_1V2

USB_1V2

UC5 1u/4/X5R/6.3V/K

3VDUAL

XTALO_USB3

UR8 5M/4/X

UX1

25M/20p/30ppm/49US/20/D

UC27 27p/4/NPO/50V/J

UC28 27p/4/NPO/50V/J

3VDUAL

UC2 1u/4/X5R/6.3V/K

3VDUAL

UC14 1u/4/X5R/6.3V/K

SSRXDP2

UC57 0.1u/4/X7R/16V/K

UC58 0.1u/4/X7R/16V/K

UC6 1u/4/X5R/6.3V/K

UC12 1u/4/X5R/6.3V/K

UR15 6.2K/4/1

3VDUAL

UC35 0.1u/4/Y5V/16V/Z

UC34 0.1u/4/Y5V/16V/Z

UC37 0.1u/4/Y5V/16V/Z

UC38 0.1u/4/Y5V/16V/Z

UC39 0.1u/4/Y5V/16V/Z

UC40 0.1u/4/Y5V/16V/Z

UC36 0.1u/4/Y5V/16V/Z

USB_1V2

UC43 10u/8/X5R/6.3V/K

UC44 1u/4/X5R/6.3V/K

UC54 1u/4/X5R/6.3V/K

UC49 10u/8/X5R/6.3V/K

UC42 1u/4/X5R/6.3V/K

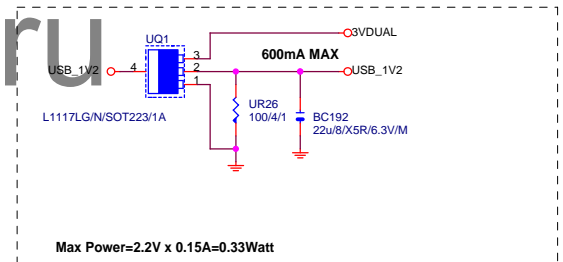
3VDUAL

EJ168

3VDUAL=550mA max

USB1V2=150mA max

www.gigabyte1.ru



AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]

GIGABYTE

Title

F_USB3.0 EJ168

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1.3

